

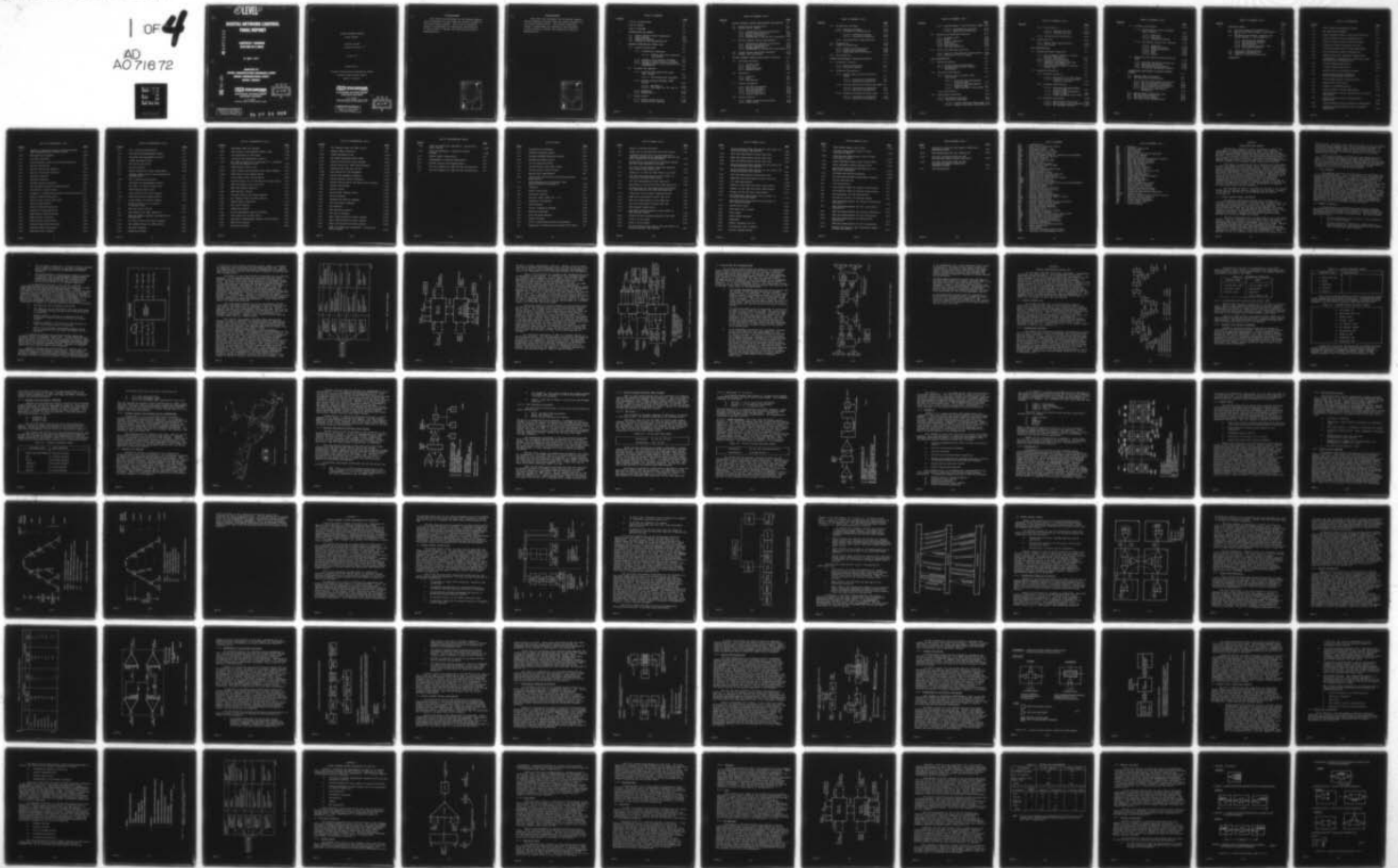
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GTE SYLVANIA INC NEEDHAM HEIGHTS MASS ELECTRONIC SYS--ETC F/G 17/2  
DIGITAL NETWORK CONTROL.(U)  
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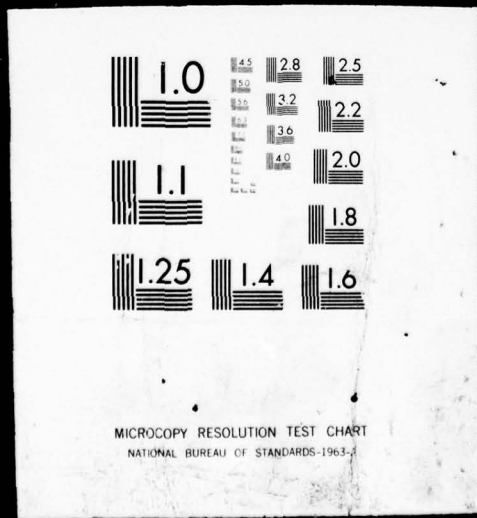
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# **DIGITAL NETWORK CONTROL FINAL REPORT**

AD A 071 672

**CONTRACT NUMBER  
DCA100-76-C-0064**

**27 MAY 1977**

**SUBMITTED TO  
DEFENSE COMMUNICATIONS ENGINEERING CENTER  
DEFENSE COMMUNICATIONS AGENCY  
RESTON, VIRGINIA**

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INCORPORATED  
**ELECTRONIC SYSTEMS GROUP  
EASTERN DIVISION**

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DIGITAL NETWORK CONTROL

FINAL REPORT

Contract Number

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Submitted to

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Reston, Virginia

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# ACKNOWLEDGMENT

This effort was performed for the Defense Communications Engineering Center under the helpful guidance of the System Control Branch. GTE Sylvania especially wishes to acknowledge the cooperation and assistance of Major Gordon S. Bounds, the Contracting Officer's Representative.

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# LIST OF ACRONYMS

AII	-	AUTOSEVOCOM II
ACOC	-	Area Control Operations Center
A/D	-	Analog to Digital
ADMU	-	Data Memory Unit in IRGA
AOCU	-	Output Control Unit in IRGA
ARF	-	Alarm Reporting Functions
ASCII	-	American Standard Code for Information Interchange
ATEC	-	Automated Technical Control
BCI	-	Bit Count Integrity
BDMU	-	Data Memory Unit in IRGB
BER	-	Bit Error Rate
BITE	-	Built In Test Equipment
BOCU	-	Output Control Unit in IRGB
B/S	-	Bits per Second
CAML	-	Connection Address Memory Load
CCU	-	Central Control Unit
CEG	-	Common Equipment Group
CIF	-	Communications Interface Function
CIS	-	Communications Interface Set
CNCE	-	Communications Nodal Control Element
COMSEC	-	Communications Security
CONUS	-	Continental United States
CPMAS	-	Communications Performance Monitoring and Assessment
CPU	-	Central Processing Unit
CRT	-	Cathode Ray Tube
CSTS	-	Combined Space-Time Switching
CTF	-	Controller Terminal Function
DAU	-	Digital Applique Unit
DAX	-	Digital Access Exchange
DCA	-	Defense Communications Agency
DCAC	-	Defense Communications Agency Circular
DCAOC	-	DCA Operations Center
DCE	-	Digital Control Element
DCEC	-	Defense Communications Engineering Center
DCS	-	Defense Communications System
DEB	-	Digital European Backbone
DMA	-	Digital Multiplex Applique
DMU	-	Data Memory Unit
DOCC	-	DCA Operations Control Complex
DOD	-	Department of Defense
DRAMA	-	Digital Radio and Multiplexer Acquisition
DSDS	-	Digital Space Division Switching
DTDS	-	Digital Time Division Switching
FDM	-	Frequency Division Multiplex
FKV	-	Frankfurt-Koenigstuhl-Vaihingen
FM	-	Frequency Modulation
IFCU	-	Input Framing and Conversion Unit
IFU	-	Input Framing Unit
I/O	-	Input/Output
IRGA	-	Interface and Reassignment Group A
IRGB	-	Interface and Reassignment Group B



LIST OF ACRONYMS (Cont.)

KBD	- Keyboard
KDU	- Keyboard Display Unit
KG	- Key Generator
LOS	- Line of Sight
MAS	- Measurement Acquisition Subsystem
MB/S	- Megabits per Second
MBS	- Mission Bit Stream
MTBC	- Mean Time Between Catastrophic Failures
MTBF	- Mean Time Between Failures
MTBI	- Mean Time Between Incidents
MTTR	- Mean Time To Repair
MTU	- Master Tuning Unit
NCS	- Nodal Control Subsystem
OCU	- Output Control Unit
OFCU	- Output Framing and Control Unit
OFU	- Output Framing Unit
PCM	- Pulse Code Modulation
PROM	- Programmable Read-Only Memory
PSU	- Power Supply Unit
RAM	- Random Access Memory
ROM	- Read Only Memory
SCBS	- Service Channel Bit Stream
SCS	- Sector Control Subsystem
SDMU	- Data Memory Unit in SRS
SDS	- Software Directed Switching
SOCU	- Output Control Unit in SRS
SRS	- Subchannel Reassignment Subsystem
SYSCON	- System Control
TCCF	- Tactical Communications Control Facility
TCF	- Technical Control Facility
TDM	- Time Division Multiplex
TMR	- Triple Modular Redundancy
VDU	- Visual Display Unit
VF	- Voice Frequency

## SECTION 1

### INTRODUCTION AND SUMMARY

GTE Sylvania, Eastern Division, is pleased to submit this Final Report on Digital Network Control (DNC). The study was performed for the Defense Communications Engineering Center under contract DCA100-76-C-0064 during the eleven month period July 1976 to May 1977. The analyses, results and conclusions contained herein are in accordance with the objectives of the eight SOW Tasks and fully address the requirements, benefits, application, and implementation of DNC with respect to the European Defense Communications System.

This report is organized so that it parallels the progression of effort performed during the study. This is done for clarity and ease of comprehension of the subject matter. Section 2 describes the present and planned European DCS and provides the basis for subsequent DNC concept development. Section 3 establishes the requirements and benefits of DNC and Section 4 examines the optimal application of DNC to the DCS so as to maximize the derived benefits. Sections 5 and 6 determine the preferred technology and control procedures for realizing DNC and Section 7 discusses in detail a conceptual implementation of the hardware and software. Section 8 provides an illustrative application of DNC to a selected segment of the DCS, and Section 9 presents unit production cost estimates for the modular building blocks comprising DNC hardware.

The remainder of Section 1 provides an overview of the related background, the approach used to accomplish the SOW Tasks, a summary of the results, conclusions, and recommendations for further investigation.

#### 1.1 DIGITAL NETWORK CONTROL BACKGROUND

The Defense Communications System (DCS) satisfies the long-haul communications needs of the Department of Defense (DoD). It includes a worldwide complex of terrestrial (LOS, coaxial, tropo, HF) and satellite transmission facilities, circuit-switched and store-and-forward common user and specialized networks, and system control facilities. The DCS also permits interoperability with other communications systems by providing all necessary control and equipment interfaces. Examples of these other systems are NATO, TRI-TAC and the various commercial systems.

The basic transmission unit in today's DCS is the 4 kHz analog channel. Both the transmission and switched networks are geared to providing capacity in terms of this basic unit, e.g., FDM groups, supergroups and mastergroups, and AUTOVON interswitch trunks. The DCA is presently implementing transmission upgrades such as the Frankfurt-Koenigstuhl-Vaihingen (FKV) and Digital European Backbone (DEB) Phase 1 program, and planning future transmission and switching upgrades such as DEB Phases 2, 3 and 4 and AUTOSEVOCOM II. These upgrades are part of a planned conversion from an all analog to an all

digital plant. Concurrent with these activities, the DCA will modify its system control capabilities. This is necessary to ensure the continuity and performance levels of DCS service during the transitional phases of DCS operation and to correct known control deficiencies which would be severely aggravated by the growing complexity of the DCS.

Within this framework, the specific task addressed by this report is to identify and analyze the additional system control capability, collectively labeled DNC, made necessary by the evolving DCS. In particular, the necessity and benefits derived from DNC must be clearly demonstrated with respect to performance of the digital European DCS, the effectiveness of system control, and DCS interoperability with other communication systems.

## 1.2 STUDY APPROACH

The approach used within the DNC study is in accordance with the following methodology. First, the capability of the present and planned European DCS was defined in order to provide a baseline for establishing DNC requirements. Included was an examination of the capability and required performance levels of transmission and switching systems and a complete analysis of the role played by system control. Second, the system control flexibility required to meet changing requirements brought about by system upgrades both within and outside the DCS was examined. Of particular interest are any necessary time constraints, the increasing need for real-time control, and interfacing problems related to AUTOSEVOCOM II and TRI-TAC. Next, DNC requirements and related DCS performance benefits were extracted from the baseline DCS and system control concepts developed. Finally, DNC hardware and software were conceptually designed including an investigation of the level of application, criteria for deployment, applicability of existing hardware, system control integration and impact on DCS operation, maintenance, and performance.

## 1.3 SUMMARY OF RESULTS

An evaluation of the planned DCS system control subsystem indicated control deficiencies in the areas of transmission capacity utilization, network reconfiguration capability, network flexibility, and AUTOSEVOCOM II and TRI-TAC interoperability. The major problems identified include:

- a. Circuit backhauling - which results in the inefficient use of circuit mileage.
- b. Limited restoration capabilities - due primarily to complicated and time consuming procedures and a general lack of compatible, spare channels.



- c. Loss of network flexibility - resulting from an increase in the number of channels in the basic transmission group cross-section which accompanies the digital upgrading.
- d. TRI-TAC/AUTOSEVOCOM II/Transmission backbone interface limitations - due to submultiplexer inefficiencies, incompatibilities between TRI-TAC formatted digital groups and T1 digital groups, and an inability to utilize the AN/TTC-39 at its designed capability.

It was determined that DNC in the form of a channel reassignment capability and associated control mitigates and in many cases eliminates the deficiencies discussed above. Channel reassignment as described here denotes the ability to assign the data in a time slot of a digital group to another time slot in the same or different digital group whether the groups be composed of PCM/TDM or 16/32 kb/s channels. Figure 1-1 illustrates this concept. As may be seen in this figure, the result of a channel reassignment is equivalent to a patching operation performed at the channel level. However, the advantages to be gained by performing a channel reassignment as opposed to a patching operation include the following:

- a. The operation can be remotely controlled.
- b. The operation can be performed at stations where there is no channel breakout and thus where channel patching is impossible.
- c. Several channels, a group or a supergroup can be reassigned as rapidly and as accurately as a single channel.
- d. Automatic feedback of the status of the operation to higher level system control is achieved.
- e. Control of the channel reassignment hardware can be easily integrated into the future DCS system control structure.

A comparative analysis was performed between manual and automated channel reassignment capabilities. It was determined that automated control is preferred. The basic reasons for this are that a manual capability fails to realize the reassignment advantages listed above and in fact provides no significant benefits over the planned system control subsystem unaugmented by DNC. Whereas, an automated capability fully realizes each of the advantages.

DNC also provides operational benefits to the DCS other than those related to the system control deficiencies. These benefits include the capability to rapidly restore high priority circuits, the provision of means for DCS transmission control to perform performance assessment and fault isolation in digital circuits, and the ability,



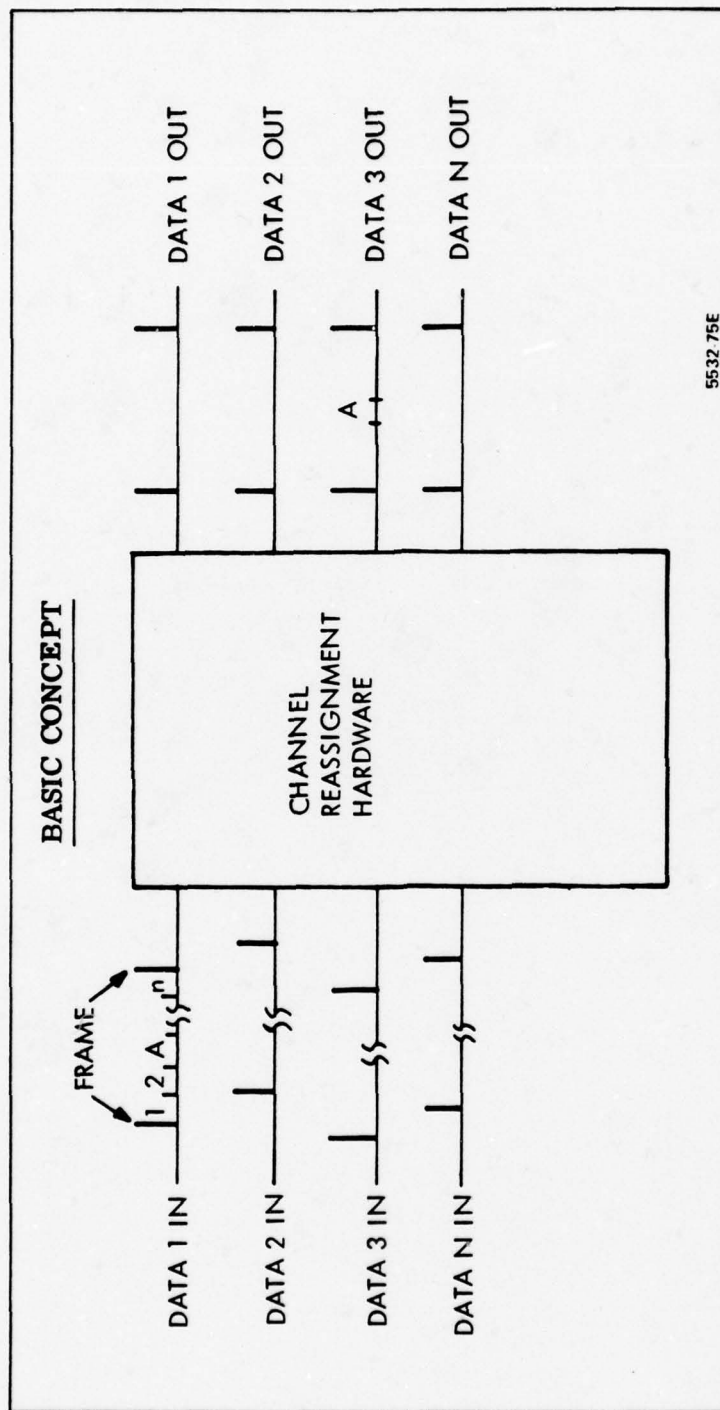


Figure 1-1. Basic Channel Reassignment Concept

in conjunction with Automated Technical Control (ATEC), to automate the technical control functions at unattended DCS stations. Figure 1-2 summarizes the relationship between automated DNC, its types of applications within the DCS, and the overall benefits the DCS derives from its application.

The manner in which DNC should be integrated into the DCS was analyzed. It was determined that the preferred location of DNC hardware within the DCS transmission hierarchy is the digital group level. The other hierarchical alternatives are unacceptable because of the constraints they place on DNC applicability and hardware realization problems. The modularity of DNC hardware with respect to function and size was investigated. The key result is that the hardware must separately process byte-interleaved channels (as contained within T1 digital groups) and bit-interleaved channels and subchannels (as contained within TRI-TAC formatted digital groups such as used in AUTOSEVECOM II). Figure 1-3 illustrates the chosen modularity. In this figure, the DNC A function and the DNC B function perform, respectively, the reassignment of byte-interleaved channels and bit-interleaved channels and subchannels. Either function is capable of stand-alone operation.

The relationship between the various DCS upgrades and DNC requirements and capabilities was examined in order to determine the time frame in which DNC would be applicable to the DCS. Results indicate that DNC could be deployed no earlier than 1978, which is the planned interim operational capability for DEB Stage II, and that the deployment is principally constrained by the requirement for a suitable timing network. However, such a timing structure would be available about 1984 and probably sooner.

Four channel reassignment techniques were evaluated and compared in order to determine the optimal methods for implementing the DNC-A and DNC-B functions. The alternatives considered include digital space division switching, digital time division switching, software directed switching, and combined space-time switching. The alternatives were compared with respect to cost, reliability/maintainability/availability, control complexity, modularity, size, and power. The analysis was first performed for the DNC-A function and the results extrapolated to the DNC-B function. It was determined that digital time division switching is the preferred approach for both cases. This approach has the lowest equipment costs, best R/M/A, and simplest control algorithms of the four techniques. Various commercial and military equipments which perform digital time switching were evaluated in order to determine if they can satisfy DNC functional requirements. With respect to the DNC-A function, it was found that existing hardware provides many more functions such as signaling, routing, etc., than required for the DNC application. This results in significantly greater hardware and software costs than is necessary to perform channel reassignment. Therefore, it was recommended that the study proceed with the conceptual design of hardware to perform the DNC-A function. With respect to the DNC-B function, the only applicable hardware is the

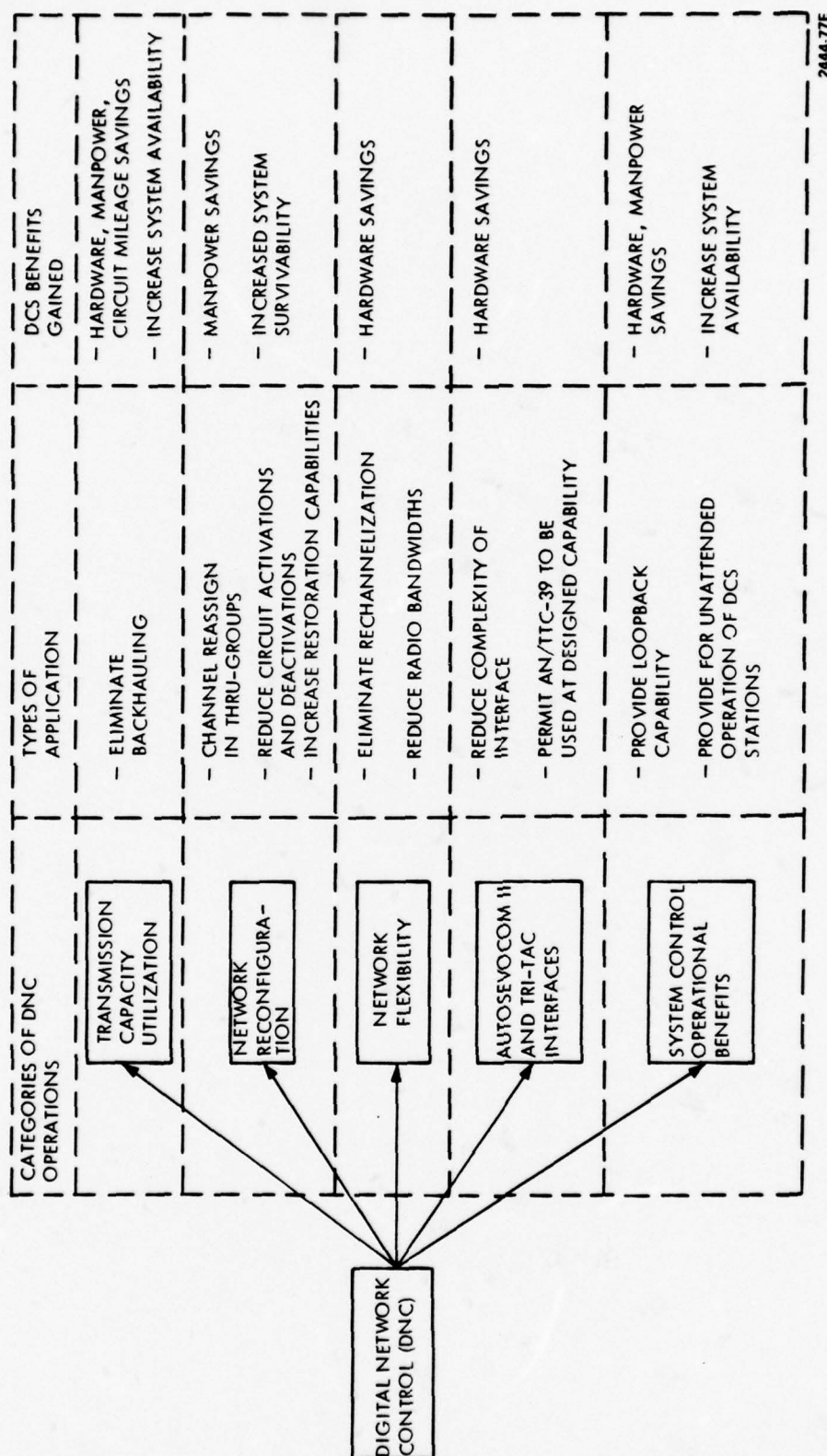
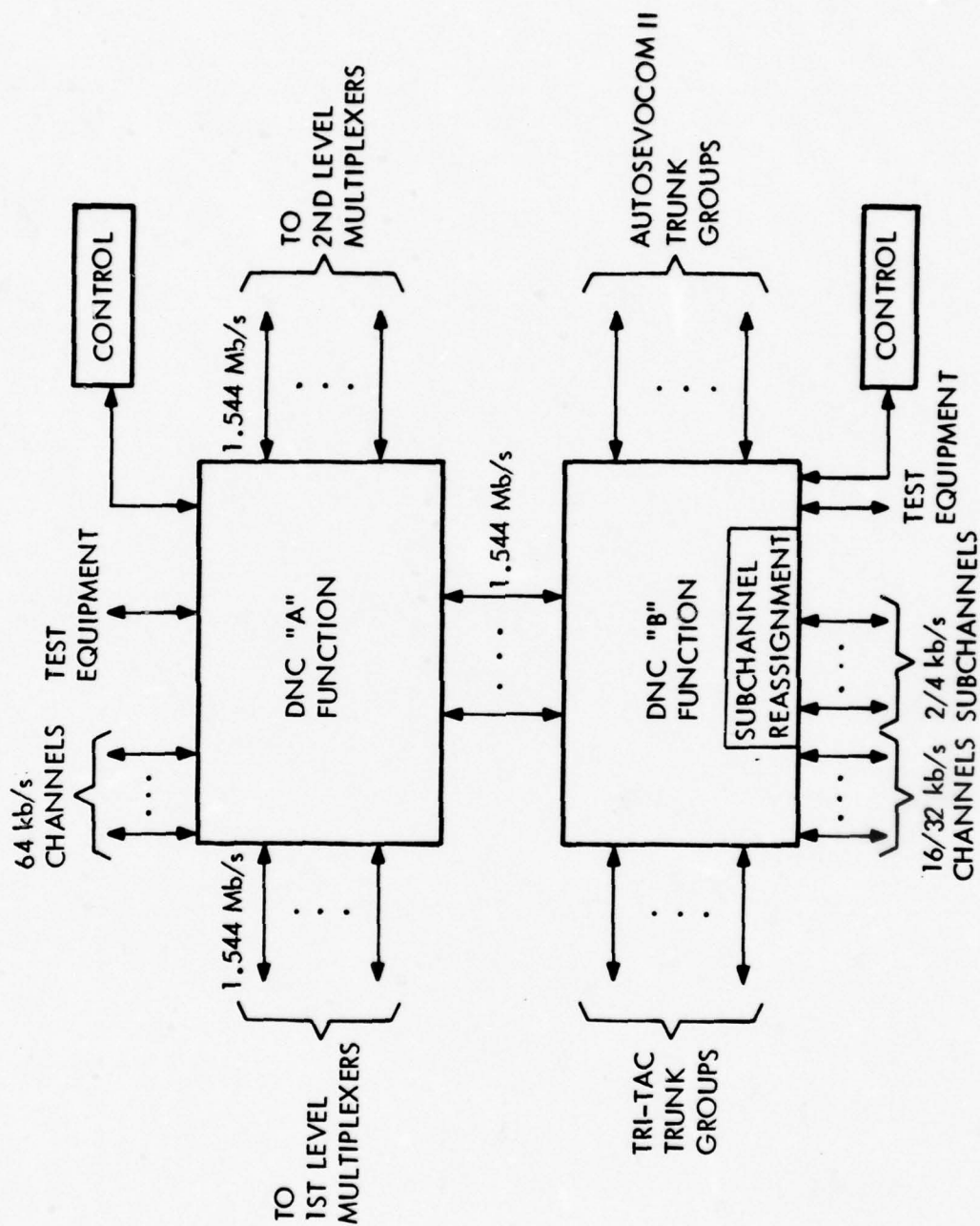


Figure 1-2. DNC Application Summary



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Figure 1-3. Digital Network Control Functional Modularity

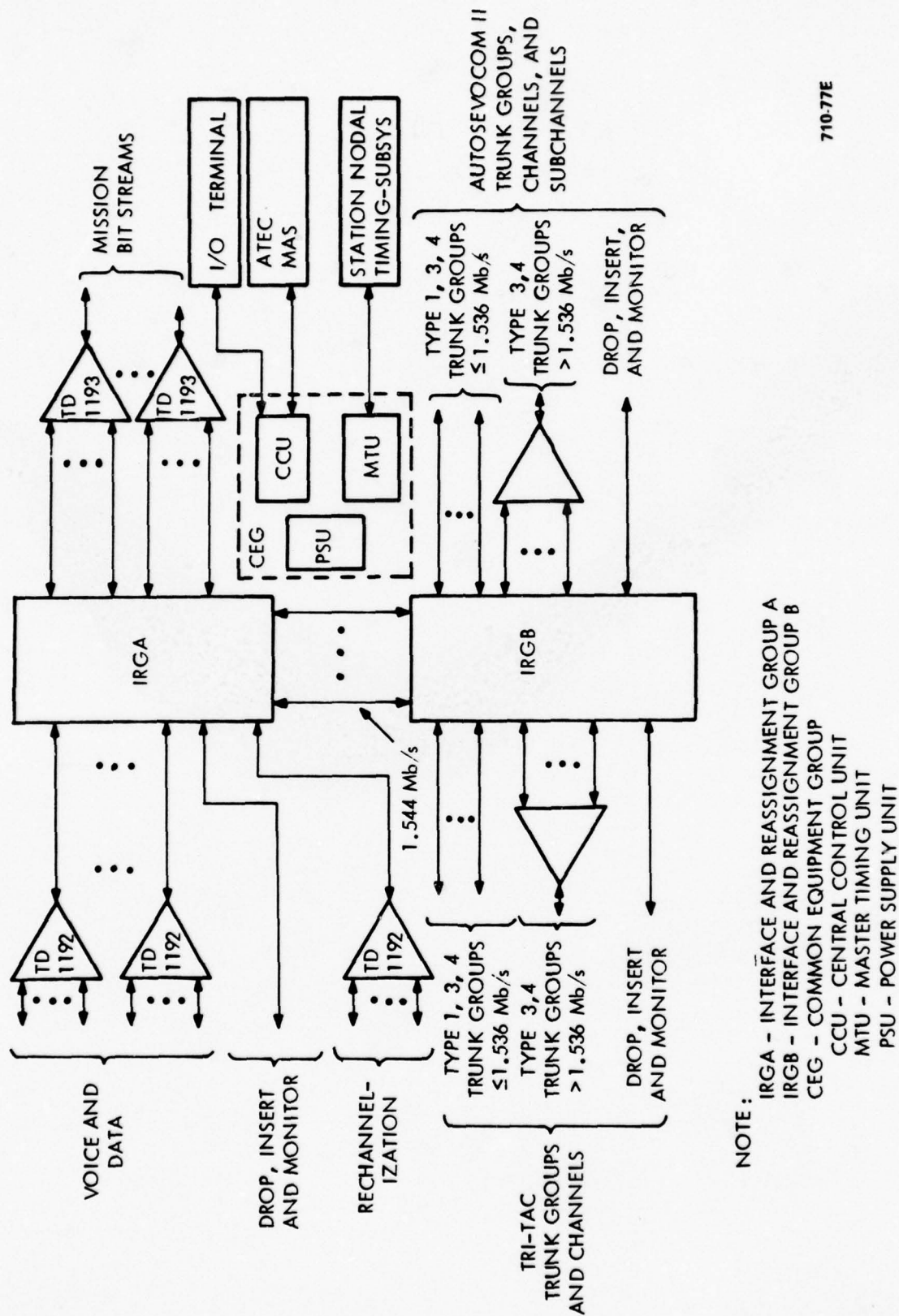


AN/TSQ-111 channel reassignment function. However, there are major interfacing problems associated with using this TRI-TAC device in the DCS. As a result, it was recommended that hardware be developed to perform the reassignment of bit-interleaved channels and subchannels.

Figure 1-4 illustrates the conceptual DNC implementation as it is deployed at a ECS station. It consists of three hardware groups: the Interface and Reassignment Group A (IRGA), the Interface and Reassignment Group B (IRGB), and the Common Equipment Group (CEG). The IRGA provides interfacing and reassignment of 64 kb/s byte-interleaved channels (satisfying the DNC-A function), the IRGB handles 16 and 32 kb/s channels and 2 and 4 kb/s subchannels (satisfying the DNC-B function), and the CEG provides functions common to both the IRGA and IRGB such as power and tuning. The DNC hardware deployed at a station is collectively labeled a Digital Control Element (DCE). The CEG is required for all DCEs, whereas the IRGA and IRGB are optional. A DCE may be configured to have only a IRGA, a IRGB or both. Which equipment would be deployed is determined by both network and station requirements. The DCE is also modular in size. The IRGA is expandable in blocks of 32 T1 digital groups up to maximum of 192 T1 groups, the IRGB is also modular and provides for a maximum capacity of 50 TRI-TAC formatted groups.

Functional control of the DCE hardware is distributed between the CEG CCU and the software located at the system control node and sector levels. The software which interfaces the DCE with system control personnel is located in the Nodal Control Subsystem (NCS) and the Sector Control Subsystem (SCS) of ATEC because this places it closer to the point where most control decisions are made. This is beneficial since it permits easy access to the ATEC data base located in an NCS or SCS. The DCE control software will need the information in the data base therefore, colocating the two eliminates the need for a duplicate data base for the DCE. Alternatively, this software could run on the CCU and access the nodal data base via the ATEC communications facilities, but this approach would result in a higher load placed on these facilities by the DCE than if this software were colocated with the data base. Also, the DNC software in the NCS and SCS can share some software with ATEC, such as data base and I/O routines.

An illustrative application of DNC to a selected segment of the DCS was performed. Five DNC deployment alternatives were examined with respect to the degree of network routing flexibility provided, hardware size and complexity, and acquisition costs. The preferred alternative, Full Flexibility, permits a channel to be automatically established between any two first-level multiplexer ports in the network and provides the circuit control to dynamically alter its routing. DNC also provides the capability to remotely exercise this control from associated sector, nodal or station levels.



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Figure 1-4. Digital Network Control Implementation

#### 1.4 CONCLUSIONS AND RECOMMENDATIONS

This study has demonstrated that augmenting the planned DCS system control subsystem with automated DNC results in additional control capabilities which minimize and in many cases eliminate existing DCS control deficiencies. In addition, DNC also provides numerous operational performance benefits which are advantageous for their potential to decrease DCS O&M costs and increase network availability and survivability. For these reasons it is recommended that DNC should be integrated into the future DCS system control subsystem. It is also recommended, however, that three areas receive further study as a means of determining the optimum application of DNC to the DCS. These areas are discussed below.

- a. A prototype development program which would evaluate the DNC concept through hardware and control software implementation is recommended. The DNC Field Test Model shown in Figure 1-5 provides the means to evaluate the capabilities of automatic DNC in a transmission system field environment. The test control processor in the field test model controls the DCEs at both the local and remote sites. Remote control of the DCS at Site B is accomplished via a service channel multiplexer telemetry channel.

The Field Test Model could be configured to include only an IRGA or both an IRGA and an IRGB. The former would provide the capability to completely evaluate the impact of DNC on DCS operations and control capabilities with respect to the DCS transmission subsystem. The joint deployment of an IRGA and IRGB would also permit the evaluation of DNC in providing interoperability with TRI-TAC and AUTOSEVOCOM II. Because of the modularity of the DCE design, the IRGBs can be deployed subsequent to the IRGAs without hardware changes to the initial test configuration.

- b. In an environment consisting of an automated technical control ATEC capability and a DNC capability, the procedures for circuit restoral/alternate routing must be strictly defined. The ability to restore circuits and wideband facilities increases with the application of automated techniques. Procedures are required which permit the correlation of the current status of the network with stored restoration plans and which permit the dynamic calculation of restoration plans should the desired routes be unavailable. With ATEC providing automated network assessment and DNC providing automated restoration/alternate routing, the connectivity data bases of the two systems must be efficiently organized. Efficient data base organization will permit smooth integration of these system control automated capabilities.



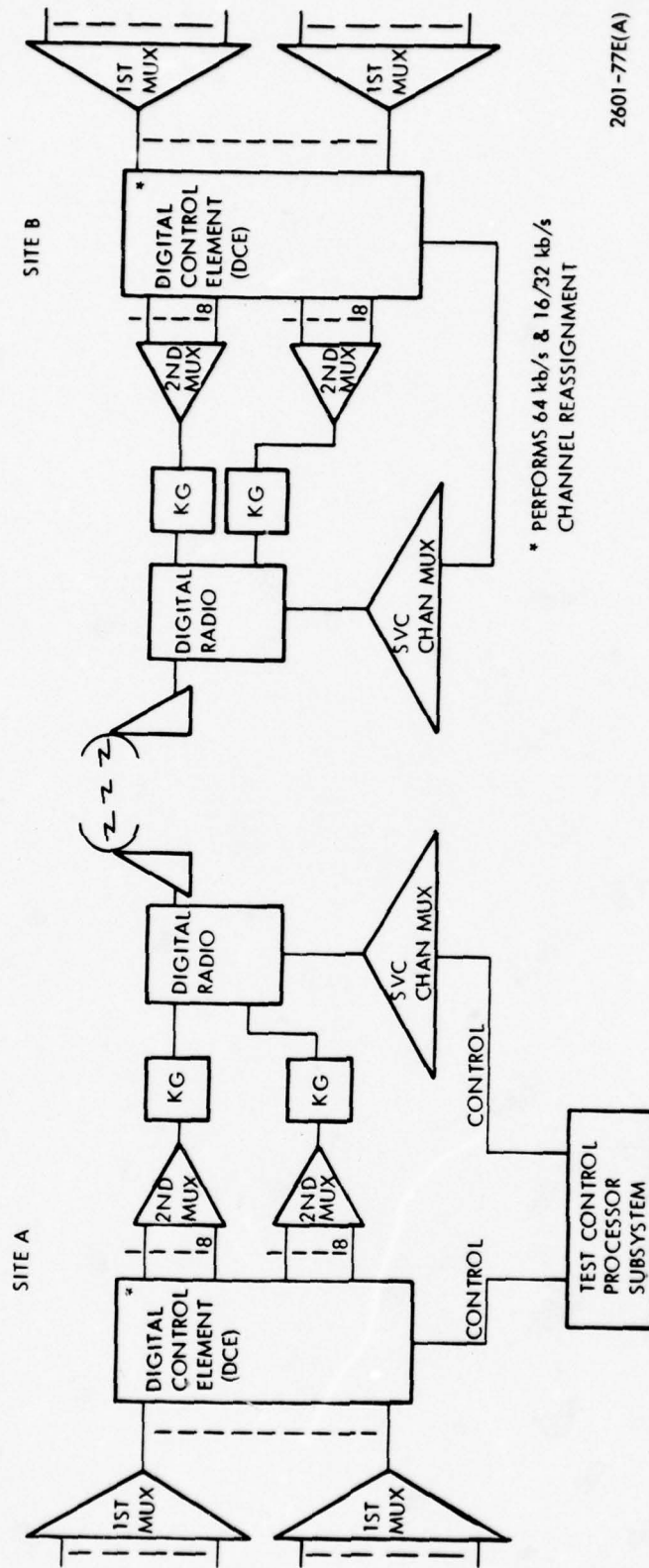


Figure 1-5. Digital Network Control Field Test Model



It is recommended that a study addressing these issues be performed. The scope of work should consist of organizing the connectivity data bases at all system control hierarchical levels, determining data base update procedures and controls, and developing the back-up recovery procedures necessary to assure desired system operation.

- c. DCS performance enhancement derived from DNC makes it extremely advantageous to consider including some or all DNC functions in the future DCS system control subsystem. However, the decision making process must consider the cost of these benefits. Specifically, DCS system control benefits and related cost benefits derived from DNC must be traded-off against life cycle costs associated with the various deployment options.

It is proposed that a study effort be undertaken to establish the cost-effectiveness of augmenting system control with an automated DNC capability. The functions, applications and engineering of DNC elements used as inputs to this analysis will be based upon the results of this DNC study.

## SECTION 2

### DEFENSE COMMUNICATION SYSTEM (DCS)

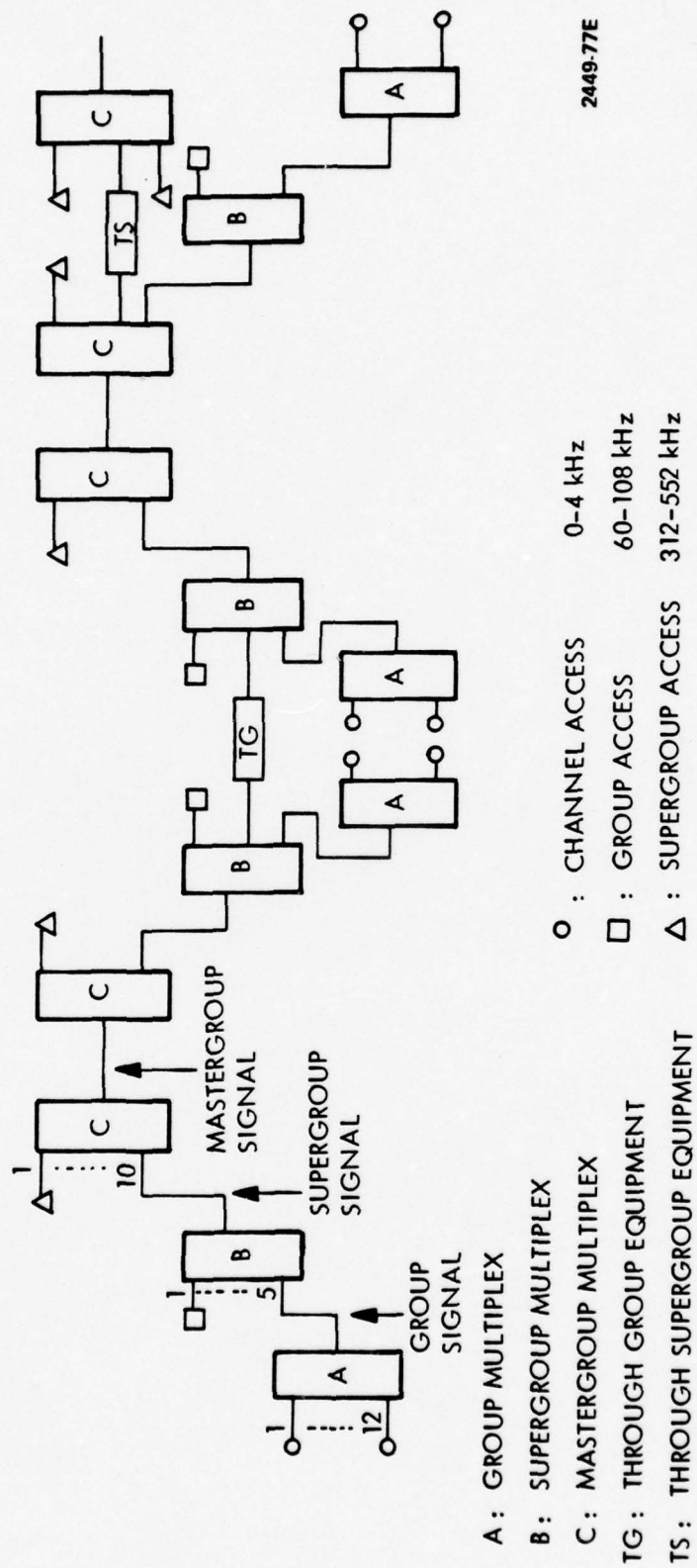
The DCS today comprises three major subsystems: transmission, switching, and system control. The transmission and switching subsystems provide the facilities to satisfy the vast majority of the voice, facsimile, and record communication needs of the DoD. The system control subsystem ensures that end-to-end performance objectives are maintained during day-to-day operation. Because of the growing complexity of the DCS and the increasing traffic demands being placed upon it, the DCA is presently implementing and planning upgrades to the DCS to guarantee that it continues to satisfy DoD communication needs. These upgrades are generally characterized by the replacement of analog facilities with digital facilities and the introduction of new digital equipment. This is especially true in the European theater as exemplified by FKV, DEB and AUTOSEVOCOM II. The remainder of this section focuses on the European DCS in order to define the environment in which DNC will operate.

#### 2.1 PRESENT EUROPEAN DCS

The present European DCS is a communications complex consisting of long-haul and local access transmission facilities, common user and specialized networks, and a system control subsystem which is responsible for overall management and operational control. The basic transmission unit within this communications complex is the 4-kHz analog (VF) channel. Both the transmission and switched networks are geared to providing capacity in terms of this basic unit. Specific examples of this are FDM groups, supergroups and mastergroups, AUTOVON interswitch trunks, and AUTODIN VF channels. The capabilities and requirements of the present European switching and transmission subsystems is examined in more detail in the remainder of Section 2.1. A general discussion of the system control subsystem is deferred until Section 2.3.

##### 2.1.1 Transmission Subsystem

The present DCS transmission subsystem is predominantly analog and utilizes a frequency division multiplexing (FDM) hierarchy built upon the 4-kHz VF channel. Figure 2-1 illustrates the FDM hierarchy. This FDM equipment is compatible with that used by the various common carriers, tactical systems and NATO, and may be interfaced at any level in the hierarchy. Performance and interfacing characteristics of FDM equipment are described in detail in MIL-STD-188-100 and will not be discussed here. Digital data transmission through the analog FDM hierarchy is accomplished by converting the data, via modems, to quasi-analog form (see MIL-STD-188-100, Section 4.1.2.3.3). Narrowband data (<9600 b/s) can be handled by modems placed at the VF channel level. Wideband data requires modems operating at the group or supergroup level.



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Figure 2-1. Frequency Division Multiplex Hierarchy



Transmission in the DCS is accomplished by using either metallic lines or radio. Table 2-1 lists the common techniques used in both categories. Within the European theater, the primary long-haul transmission technique is LOS radio.

TABLE 2-1. TRANSMISSION TECHNIQUES

METALLIC LINES	RADIO
- Twisted pair cable	- Line of Sight (LOS)
- Multipair cable	- Troposcatter
- Coaxial cable	- Satellite
	- High Frequency (HF)

#### 2.1.1.1 Defense Satellite Communications System (DSCS)

DSCS provides long-haul transmission for the DCS via satellite relay. DSCS is being upgraded in phases and is presently operating under Stage IB of Phase II. Phase II satellites will be placed in geostationary orbits and will therefore be continuously available from earth terminals within their operational range. Fixed earth terminal locations in the European area include Landstuhl and Coltano.

Stage IB of DSCS provides a multipoint network capability via FDMA and employs spread spectrum modulation for secure point-to-point communications. The earth terminals utilize FDM/FM techniques and have a maximum modem capability of 72 VF channels.

#### 2.1.2 Automatic Voice Network (AUTOVON)

AUTOVON is the DoD's worldwide communication system for providing VF circuit-switched service. Although its primary mission is to provide non-secure voice service, it also provides backup service for AUTODIN and AUTOSEVOCOM. The major difference between AUTOVON and the various commercial circuit switch services is that it incorporates a system of precedence designations and preemption protocols. Within this system, high precedence callers can preempt lower precedence callers in order to prevent blocking of the former. The levels of precedence used in AUTOVON are shown in Table 2-2 in decreasing order of precedence.



TABLE 2-2. AUTOVON PRECEDENCE LEVELS

PRECEDENCE LEVEL	SUBSCRIBER KEY
1. Flash Override	FO
2. Flash	F
3. Immediate	I
4. Priority	P
5. Routine	-

There are 17 overseas AUTOVON switches of which 10 are located in the European theater as shown in Table 2-3. The AUTOVON switching centers may include technical control equipment, automatic switching equipment, and Dial Service Assistance (DSA) operator positions.

TABLE 2-3. EUROPEAN AUTOVON SWITCHING CENTERS

1. Hillingdon, GB
2. Martlesham Heath, GB
3. Humosa, Spain
4. Coltano, Italy
5. Mt. Vergine, Italy
6. Mt. Pateras, Greece
7. Donnersberg, FRG
8. Feldberg, FRG
9. Schoenfeld, FRG
10. Langerkopf, FRG

Transmission facilities interconnecting the AUTOVON switching centers consist of the metallic and radio facilities of the DCS transmission subsystem. Transmission capacity between switches is measured in terms of 4-kHz analog interswitch trunks. AUTOVON terminal equipment must be arranged for 4-wire operation. When

subscribers are served through a 2-wire local switchboard, 2- to 4-wire conversion must be provided. AUTOVON terminal facilities include 4-wire telephones, 2- and 4-wire PBXs and PABXs, narrowband modems, and facsimile equipment.

### 2.1.3 Automatic Digital Network (AUTODIN)

AUTODIN is a switched data network providing secure worldwide communications for the DoD and other federal agencies. There are two primary communities of users in AUTODIN: strategic and intelligence tributaries. Traffic exchanges between the two is prevented. There are a total of 18 AUTODIN Switching Centers (ASCs) worldwide, 9 in CONUS and 9 overseas. Of the 9 overseas ASCs, three are located in the European theater as follows:

- a. Croughton, GB
- b. Pirmasens, FRG
- c. Coltano, Italy.

The three European locations are fully interconnected by 2400 b/s interswitch trunks with protection provided via dial-up to AUTOVON. Subscriber access lines operate at up to 2400 b/s for synchronous transmission, and up 150 b/s for asynchronous operation.

The European ASCs provide only store-and-forward service; that is, each ASC must verify and store each message before forwarding it. AUTODIN uses a system of precedences for determining the order of message processing at each switch. Table 2-4 lists the six precedence levels and the associated system objectives for cross-network delay.

TABLE 2-4. AUTODIN PRECEDENCE LEVELS

PRECEDENCE LEVEL	DELAY OBJECTIVE
CRITIC and MultiCRITIC	5 minutes maximum
ECP	5 minutes maximum
Flash	10 minutes maximum
Immediate	30 minutes maximum
Priority	3 hours maximum
Routine	6 hours maximum

The European ASCs have three basic configurations:

- a. 50 to 100 terminated lines
- b. 120 to 200 terminated lines
- c. 85 to 150 terminated lines (modification to a or b).

Each ASC includes an Automatic Digital Message Switch (ADMS), patch and test facilities, station timing source, modems and cryptographic equipment. The basic functions performed by each switch include format conversion, code conversion, routing, message security, error control, and record maintenance.

#### 2.1.4 Automatic Secure Voice Communications (AUTOSEVOCOM)

AUTOSEVOCOM is a circuit-switched network providing a worldwide secure voice communication capability. In the European theater, two primary types of secure voice service are offered. One uses narrowband subscriber terminal equipment and AUTOVON as the switching network; the other uses wideband terminal equipment and a switching network comprised of AN/FTC-31 wideband switches and interwitch trunks derived from the DCS transmission subsystem. The European wideband switch locations are Vaihingen, FRG; Ramstein, FRG; Heidelberg, FRG; and London, GB.

Narrowband service is offered at two rates, 2400 b/s via the HY-2 vocoder and 9600 b/s via the HY-11 CVSD terminal. Wideband service is provided via the 50 kb/s KY-3 PCM terminal. Communication between wideband and narrowband terminals is accomplished by first converting back to analog (clear mode) and then re-encrypting. The call set-up procedure in the present AUTOSEVOCOM is both lengthy and complicated due to diversity of equipments and the fact the set-up operation is essentially manual.

#### 2.2 EUROPEAN DCS UPGRADES

Upgrades to the DCS are planned for the transmission, switching, and system control subsystems. The transmission subsystem in Europe will be converted from all analog to all digital. This includes the replacement of FDM equipment by TDM equipment, the use of DAUs with existing FM radios, and the introduction of digital radios. The pilot digital transmission upgrade program is the FKV Project which will provide a thinline digital backbone in southern Germany. This backbone will be extended south into Italy under Stage I of the DEB program. Additional DEB stages will extend the backbone into the United Kingdom and provide lateral spurs. All transmission upgrades utilize the same PCM/TDM hierarchy and are compatible across their interface. Figure 2-2 illustrates the European digital DCS backbone following completion of DEB Stage IV.

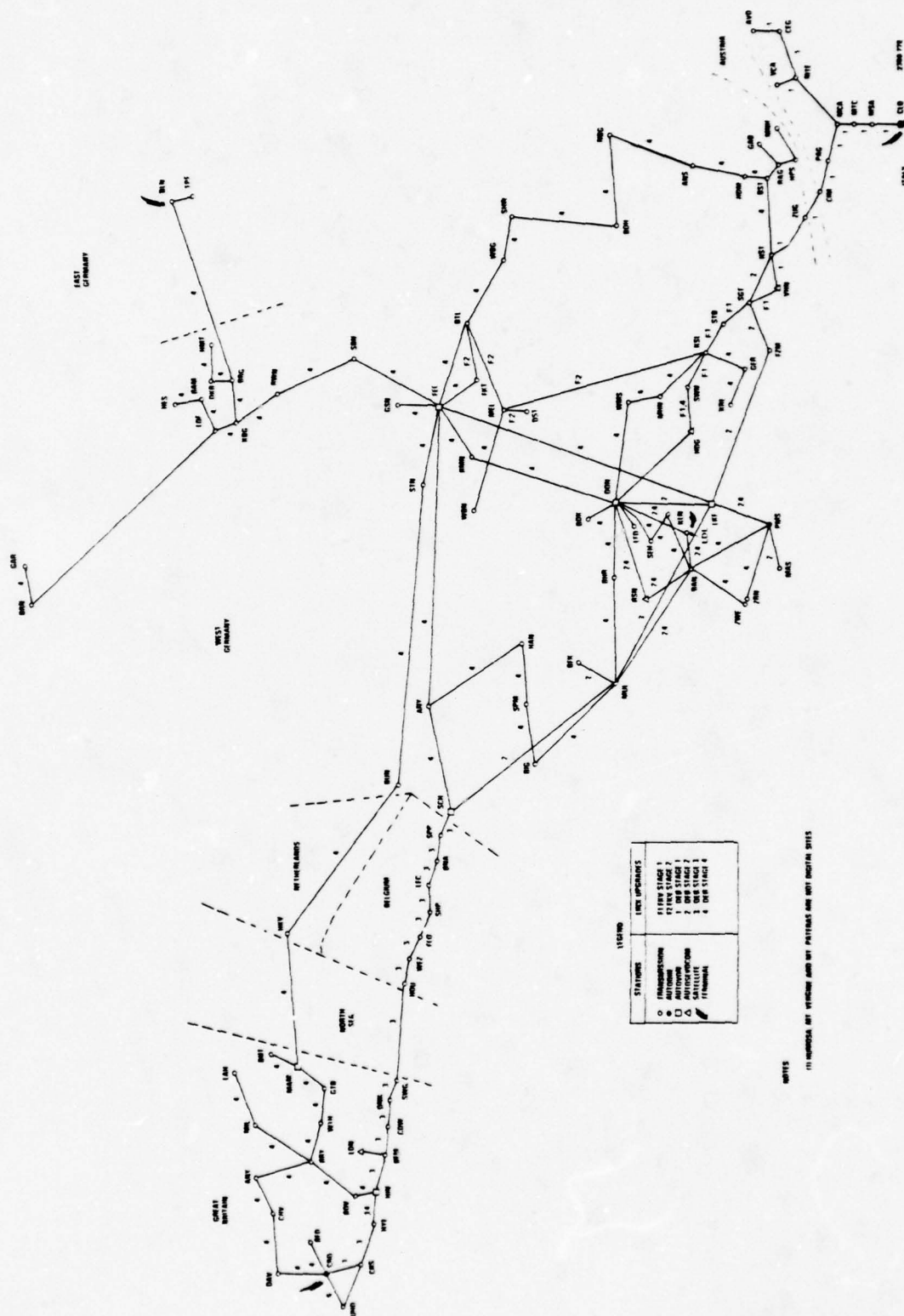


Figure 2-2. Digital European Plan Following DEB Stage 4



Planned switching subsystem upgrades are AUTOSEVOCOM II (A II) and AUTODIN II. A II is based on the use of the AN/TTC-39 circuit switch for providing both AUTOVON and AUTOSEVOCOM service. A II interswitch trunking will utilize 16 kb/s CVSD voice encoding and will be compatible with the TRI-TAC secure voice system via 16/32 kb/s conversion. However, A II will be required to provide analog 4-kHz VF service as long as the need exists. AUTODIN II, a general purpose data network which will replace the present AUTODIN, is designed to meet present and future data requirements such as man/man, man/computer, computer/computer, and computer/machine communications. Its major asset derives from the use of packet switching in place of the conventional message switching used in the present AUTODIN. Packet switching permits greater transmission efficiency and storage utilization, thereby reducing cross-network delays.

System control is undergoing modification so that it better responds to the needs of a digital environment. Although certain aspects of these modifications are well defined (e.g., the Automated Technical Control (ATEC) program), much of the future system control subsystem is still being analyzed and defined, especially in the area of overall structure and hierarchy.

#### 2.2.1 Frankfurt-Koenigstuhl-Vaihingen (FKV) Project

The FKV project is the first phase of the conversion of the European DCS to all digital. It will be implemented in two stages in southern Germany, as shown in Figure 2-2, and when complete will comprise ten nodes and nine links. Stage I which is operational provides a digital backbone from Vaihingen to Heidelberg. Stage II which is not yet operational will extend Stage I to Frankfurt via Koenigstuhl, and will also provide a lateral spur to Darmstadt.

The multiplexing hierarchy is two-level with voice access through 8-bit PCM encoding and digital data access through transitional encoding. Figure 2-3 illustrates the transmission system configuration. Secure communications are realized by bulk encrypting at the output of the first level multiplexer. All transmission is over microwave radio operating in the 8-GHz range. FM radios in conjunction with three-level partial response encoding in the second-level multiplexer provide a digital link cross-sectional capacity of 192 64-kb/s PCM channels.

Performance requirements established for the FKV project are as follows:

- a. BER - link,  $\leq 7 \times 10^{-8}$  at least 99.99 percent of the time as measured at the 12.6 Mb/s level; end-to-end (5 links maximum),  $\leq 3.5 \times 10^{-7}$  at least 99.99 percent of the time as measured at the 12.6 Mb/s level



- b. Bit Integrity - mean time to loss of bit integrity shall be greater than or equal to 24 hours from end-to-end (12.6 Mb/s to 12.6 Mb/s)
- c. Jitter - less than or equal to 1/4 of a bit period peak departure.

#### 2.2.1.1 FKV Transmission Equipment

The first-level VF multiplexer is the CY-104 which consists of three subassemblies:

- a. HY-12, 24-channel PCM multiplexer
- b. KG-34, Key Generator
- c. HN-74, Signal interface and control.

The HY-12 is a modified Vicom D2 terminal. It samples and 8-bit encodes up to 24 full duplex VF channels and then TDMS the PCM words into the standard T1 format. The KG-34 bulk encrypts/decrypts the T1 signal and the HN-74 interfaces the HY-12 with the KG-34 and the KG-34 with the T1-line. The T1WB1 is the first-level multiplexer for digital data signals in FKV. It accepts up to eight 0-50 kb/s digital signals, transitionally encodes the data, and then TDMS the codewords into the standard T1 format. Neither the CY-104 nor the T1WB1 provides redundancy.

The second-level multiplexer is the Vicom T1-4000 which TDMS up to eight full-duplex asynchronous T1 signals into a 12.56 Mb/s signal. The multiplexer is also available in two, four and six port versions with corresponding line output rates of 3.19, 6.28 and 9.46 Mb/s. Three-level partial response encoding of the line signal yields an output signal suitable for transmission over the FKV FM radios. The multiplexer is fully redundant (1:1) with automatic protection switching.

The FKV radio accepts the second-level multiplexer line signal for transmission in the 8-GHz range with an output power of one watt. The radio is fully redundant with the receivers in a space diversity configuration and the transmitters arranged for hot standby operation. The radio also provides an 8-kHz supervisory channel which is utilized for a maintenance coordination channel (0.3 - 3 kHz), MCC, and for fault alarm status reporting (FASR) (3-8 kHz).

Under the FKV FASR system, monitored functions are displayed at central locations in the TCF of major sites as well as locally. Monitored functions at unattended sites are remoted to central locations through the FASR system. The MCC supplies FKV with a link orderwire capability. Each site is capable of communicating with at least one adjacent site. Additionally, several sites are configured as a party line and one site is equipped with a remote terminal unit.



### 2.2.2 Digital European Backbone (DEB) Program

DEB is a four-stage program which will culminate in a digital transmission backbone throughout the European DCS. The first stage of DEB will extend the FKV backbone south to Italy. Stages II and III will extend Stage I west through Germany, Belgium and into the United Kingdom. Stage IV will provide an additional main line between the United Kingdom and Germany through the Netherlands, as well as provide lateral spurs on certain high priority routes. Figure 2-2 illustrates the DEB configuration as presently planned.

#### 2.2.2.1 DEB Stage I

The transmission equipment employed in DEB Stage I is similar to that used in FKV. The primary differences are discussed below.

DEB Stage I does not use the TLWB1 for digital data access. Instead, the CY-104 is provided with a special data channel card for each data channel to be accommodated, up to a maximum of 23 channels per multiplexer. Each data channel card replaces one VF channel card. The specific data rates accepted by the CY-104 are listed in Table 2-5. The line rate and transmission format of the CY-104 are unaffected by the use of data channel cards.

TABLE 2-5. CY-104 INPUT DATA RATES

Synchronous	32, 48, 56, 64 kb/s
Asynchronous	0-20, 50 kb/s

Three orderwire systems are provided in DEB Stage I, system, express and link. The link orderwire, which also serves as the MCC, utilizes the 0.3 - 2.5 kHz portion of the 8-kHz supervisory channel. The other orderwire systems replace mission channels. Monitoring of equipment at remote sites is accomplished by the Fault Alarm System (FAS). Unlike The FKV system which requires several control sites, the FAS is a master/slave type. There is a single operational master and two backup masters for reliability. All masters transmit at the same frequency although only one master is active at one time. Each remote station transmits on a separate frequency. The FAS utilizes the 3-8 kHz portion of the radio's supervisory channel.

Performance requirements established for DEB digital links are specified in terms of BER and availability. For DEB Stage I as for FKV, the link availability objective is 99.99 percent; however, the BER objective has been decreased to  $5 \times 10^{-9}$  from  $7 \times 10^{-8}$ . Requirements for subsequent DEB stages have not yet been specified.



#### 2.2.2.2 DEB Stages II, III and IV

As presently planned, DEB stages II, III and IV will employ transmission equipment procured under Project DRAMA. This equipment comprises the following:

- a. TD-1192 ( ) (P)/F, first-level multiplexer
- b. TD-1193 ( )/F, second-level multiplexer
- c. AN/FRC - ( ) ( ), digital radio.

Bulk encryption will be accomplished by the KG-81 (Walburn). There are major differences in function and configuration between DRAMA equipment and that used in FKV and DEB Stage I. Figure 2-4 illustrates the DRAMA equipment configuration. The components are discussed in Section 2.2.2.2.1.

**2.2.2.2.1 DRAMA Equipment** - The first level multiplexer is the TD-1192. It is a basic PCM channel bank and is D2/D3 and HY-12/HN-74 compatible. The multiplexer accepts both VF channels and digital data channels as input. The allowable digital data rates are listed in Table 2-6. Each digital data channel operating at less than 128 kb/s replaces a single VF channel. The 128, 256 and 512 kb/s data inputs replace, respectively, two, four and eight VF channels. In any multiplexer configuration, no more than 12 VF channels may be replaced. There are two versions of the TD-1192: a 3/6/12/24-channel and a 24-channel version. The line rates corresponding to the 3, 6, 12 channel modes of operation are 192, 384, and 768 kb/s. When operating with a full complement of 24 channels, the line rate is always 1.544 Mb/s. The first-level multiplexer is not redundant.

TABLE 2-6. TD-1192 DIGITAL DATA RATE INPUTS

Synchronous	56, 64, 128, 256 and 512 kb/s
Asynchronous	0-20 and 50 kb/s

The second-level multiplexer, TD-1193, provides for the multiplexing of up to eight digital data signals into a composite line signal with a maximum information rate of 12.352 Mb/s. The allowable set of input rates is 1.544, 3.088, and 6.176 Mb/s; they may be used in any combination as long as the total input rate does not exceed 12.352 Mb/s. When the input to the multiplexer is 3.088 or 6.176 Mb/s, the number of 1.544 Mb/s input ports utilized is two and four, respectively. The TD-1193 may be operated synchronously or asynchronously. For the latter, bit stuffing is employed in order to maintain bit count integrity. When operated synchronously, the bit stuffing is disabled and replaced by fixed rate conversion. The TD-1193 is fully redundant with automatic protection switching.

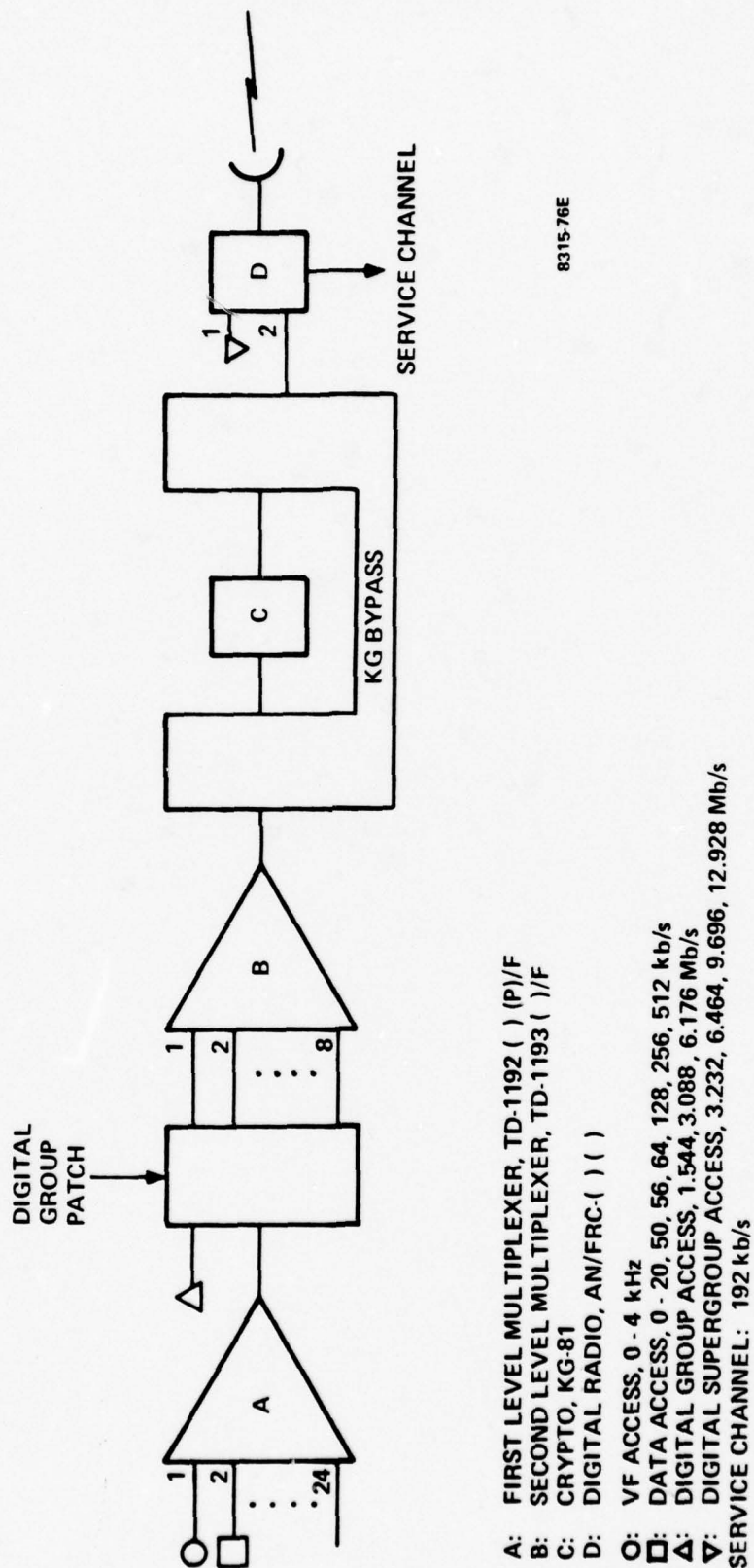


Figure 2-4. DRAMA Transmission Equipment Configuration

The AN/FRC-( ) ( ) is the DRAMA digital radio and synchronous multiplexer combination. The radio transmitter accepts one or two synchronous mission bitstreams and a digital service channel bitstream (192 kb/s), synchronously multiplexes them into a composite signal, and RF modulates the composite signal to either the 4- or 8-GHz range. The radio receiver accepts the received modulated RF carrier, and performs the inverse operations. The allowable mission bitstream rates are 3.232, 6.464, 9.696 and 12.928 Mb/s. The AN/FRC-( ) ( ) is fully redundant and incorporates automatic protection switching.

### 2.2.3 AUTODIN II

AUTODIN II is a packet-switched data network which will supplement rather than replace the present AUTODIN store-and-forward network. It will provide the additional capability required to meet the future computer communications needs of the DoD which will typically require shorter cross-network delays than are presently available through AUTODIN. AUTODIN II is a phased program. Phase I will provide a CONUS backbone packet switching network consisting of eight switches interconnected in a distributed rather than hierarchical architecture. Phase II calls for additional CONUS switches as required by traffic demand, and the introduction of a packet switching backbone in the European area.

Each AUTODIN II switch will serve both a regional and tandem function. As a regional switch, it must terminate access lines from dedicated subscriber equipment, multiplexers, and AUTODIN I ASCs. Corresponding regional functions include the following:

- a. Packetizing/depacketizing traffic to/from the backbone network
- b. Routing intra-regional messages
- c. Security checking
- d. Access line control/protocol interfacing
- e. Message accountability for messages entering or leaving the backbone network and intra-regional messages
- f. Synchronization and error control
- g. Traffic statistics gathering.

As a tandem switch, it is extensively interconnected to the other packet switches, consistent with the distributed network architecture. Corresponding tandem functions include the following:

- a. Backbone network routing of packets
- b. Interswitch trunk control
- c. Packet accountability
- d. Synchronization and error control
- e. Traffic statistics gathering.



As in AUTODIN I, a system of precedences will be employed to determine the order of message processing and allocation of resources. The AUTODIN II precedence structure, however, is more complex in that two traffic characteristics are jointly required to determine the precedence of a message. One is Application type which comprises four classes:

- a. Class A - Interactive
- b. Class B - Query/Response
- c. Class C1 - Bulk 1 or Narrative
- d. Class C2 - Bulk 2.

The other type is Criticality which has been unofficially grouped into five classes:

- a. Flash Override
- b. Flash
- c. Immediate
- d. Priority
- e. Routine.

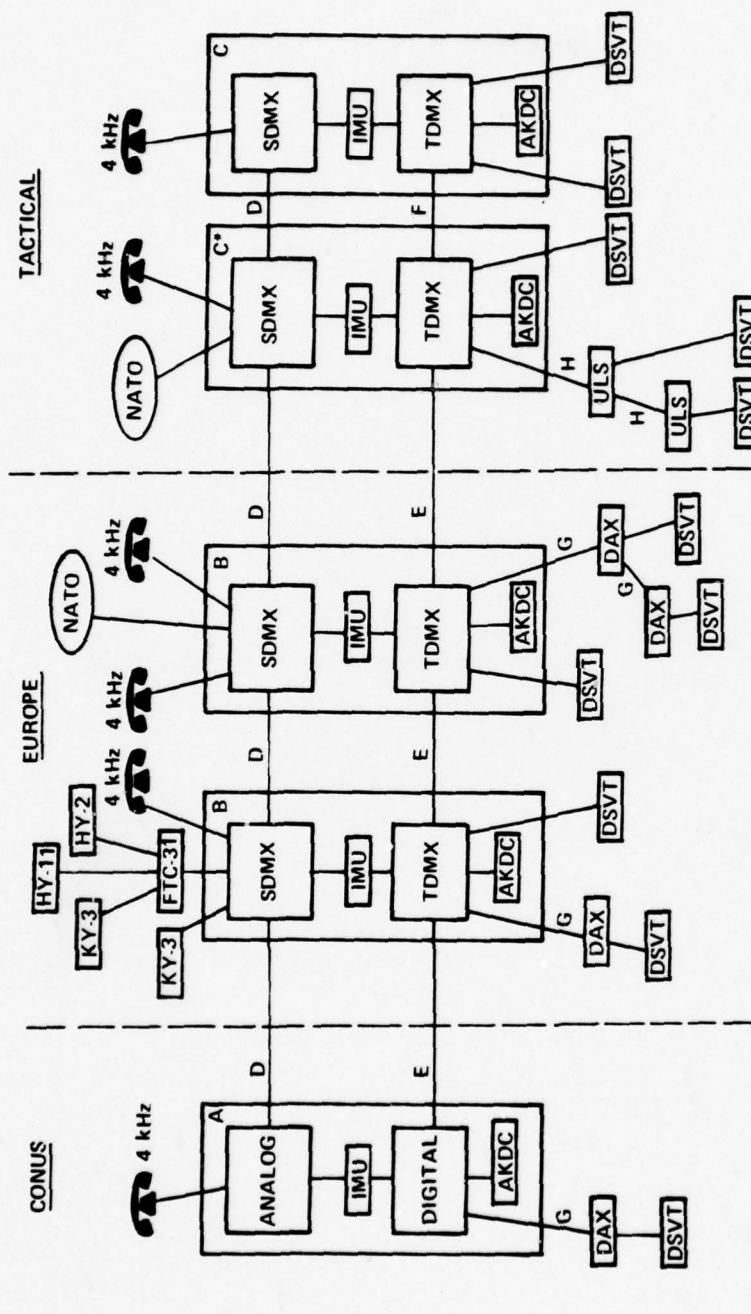
Based on Application type and Criticality, the initial AUTODIN II system will assign precedences in one of four categories. This precedence mapping will not be discussed. However, Category I which contains all Flash overrides and Flash traffic is non-blocking, consistent with normal military operations

COMSEC will be link-by-link as in AUTODIN I. Future plans call for the inclusion of automatic key distribution and end-to-end encryption as problems associated with their implementation in packet-switched networks are resolved.

#### 2.2.4 AUTOSEVOCOM II

AUTOSEVOCOM II (A II) will provide worldwide digital circuit-switched communications for the DoD. It will incorporate a multi-level automatic precedence and preemption system similar to the present AUTOVON system, as well as permit both clear voice and secure voice communications. Secure communications will be accomplished primarily through the use of the Digital Subscriber Voice Terminal (DSVT) operating at 16 kb/s. In the European theater, A II will replace the present AUTOVON and AUTOSEVOCOM systems. Backbone switching will be accomplished by AN/TTC-39s in a one-for-one replacement for the present AUTOVON switches. Additionally, access area switching will be realized by the introduction of Digital Access Exchanges (DAXs) to serve a PABX-like function. In CONUS, the AUTOVON ESS No. 1 will be modified to emulate an AN/TTC-39 switch with regard to digital subscriber and interswitch functions. Because of the nature of the A II implementation, it will be interoperable with TRI-TAC AN/TTC-39 switching with only minor interfacing. Figure 2-5





A: ESS NO. 1 MODIFIED

B: DCS AN/TTC-39

C: TACTICAL AN/TTC-39

D: ANALOG TRUNKS

E: DIGITAL TRUNKS GROUPS (INCL. CCIS), 16 kb/s CHANNELS

F: DIGITAL TRUNKS GROUPS (INCL. CCIS), 32 kb/s CHANNELS

G: DIGITAL TRUNK GROUPS (IN-BAND SIGNALLING), 16 kb/s CHANNELS

H: DIGITAL TRUNK GROUPS (IN-BAND SIGNALLING), 32 kb/s CHANNELS

IMU: INTERMATRIX UNIT

AKDC: AUTOMATIC KEY DISTRIBUTION CENTER

DAX: DIGITAL ACCESS EXCHANGE

ULS: UNIT LEVEL SWITCH

\* INCLUDES 32 kb/s TO 16 kb/s GEARDOWN CAPABILITY

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Figure 2-5. AUTOSEVOCOM II Configuration (1980 Time Frame)  
with Tactical Interoperability

illustrates the AUTOSEVOCOM configuration as it is likely to exist in the 1985 time frame. It is expected that the 1990 time frame will be characterized by all digital switching; consequently, the SDMX and analog subscriber terminals would be phased out in this era.

### 2.3 SYSTEM CONTROL

The Defense Communications System (DCS) comprises switching and transmission subsystems which are managed and operationally controlled by the DCS System Control subsystem. System control is the means whereby the DCS switching and transmission in conjunction with its O&M supervisory, administrative and management facilities, and personnel are used to maximize the communications system's performance (availability and grade/speed/quality of user service) under changing traffic conditions, natural or man-made stresses and equipment disruptions. The basic aspects of system control are:

- a. Timely acquisition of system performance data, facility and traffic load status and service quality indications
- b. Rapid analysis, processing and display of this information
- c. Subsequent decision making
- d. Execution of real-time control actions
- e. Supporting longer range system management.

System control functions are categorized as network control, traffic control and transmission control. Network control involves transmission and switched network configuration control, reconstitution/restoral of the network and extension supervision. Traffic control is concerned with maximizing the throughput of DCS traffic under changing (dynamic or gradual) traffic patterns by control of traffic flow and/or routing. Transmission control includes the quality assurance, performance assessment, fault isolation, coordination, restoral supervision/control of the trunks and circuits traversing or terminating in a transmission station. Technical Control Facilities (TCFs) and their subordinate Patch and Test Facilities (PTFs) in the DCS transmission subsystem perform these Transmission Control functions. Designated TCFs (at Reporting Stations) provide reporting upward to higher levels in the system control organization where, in conjunction with status/performance/control actions information received from the switching subsystem (AUTOVON, AUTODIN and AUTOSEVOCOM switches), performance assessment, status monitoring, etc., of more extensive portions of the DCS (regions, areas) is made available to network and traffic controllers.

### 2.3.1 Present System Control

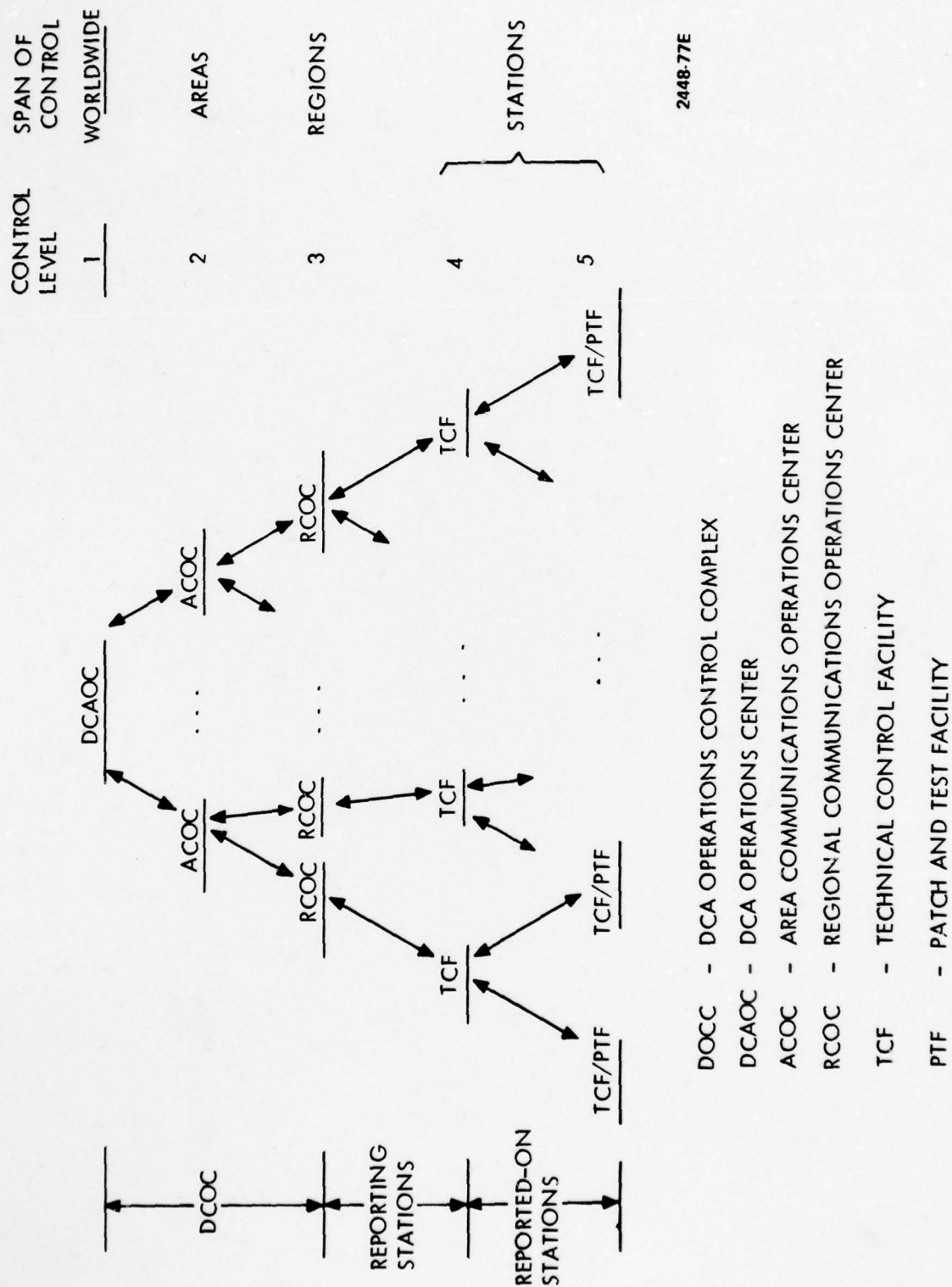
The present system control organization is shown in Figure 2-6. Control levels 1, 2, and 3 comprise the DCA Operations Control Complex (DOCC) for the DCS. Control levels 4 and 5 represent the TCF reporting stations and their associated subordinate reported-on stations. The DOCC elements, DCAOC, ACOCs and RCOCs have computer-based systems assisting in the performance of their SYSCON functions. The TCFs and subordinate TCFs/PTFs are manually operated by O & M and controller personnel of the MILDEPs. Based on information presented in DCEC Report TR 5-74 the system control system as presently constituted has a variety of deficiencies due to the non-systematic development of the system control facilities over the years.

- a. O&M Costs - excessive
- b. Duplication - data flow/file processing of information items
- c. Data Input/Control - incomplete, inaccurate, not timely
- d. Information Accessibility - slow, inadequate, voluminous files
- e. Responsiveness - slow for real-time configuration/traffic control
- f. Adaptability to support new DCS subsystems, e.g., AUTOSEVOCON II; AUTODIN II - poor
- g. Survivability/Reliability - poor.

### 2.3.2 System Control Upgrades

The planned system control organization for modernized DCS is shown in Figure 2-7. The hierarchical configuration is retained; however, the lower control levels are to be automated and their monitoring/control facilities integrated into a unified system control system that will provide each level with timely performance assessment, fault isolation and control capabilities commensurate with its hierarchical level and associated system control functions. Transmission control will be effected by control levels 3, 4, and 5. This group of control elements, Facility Control offices, Intermediate Control offices at major TCFs and subordinate TCFs/PTFs at the equipment and circuit levels within the DCS stations will be provided automated assistance under the ATEC program. At the DCS stations computer-based ATEC instrument systems will provide the monitoring, testing, status monitoring, etc., necessary for performance assessment and fault isolation. The TCF to which these stations are subordinate will contain a central processor system to control the functions of the station equipment and receive status and measurement data from them. Reporting in the hierarchy will be from TCFs (at Intermediate

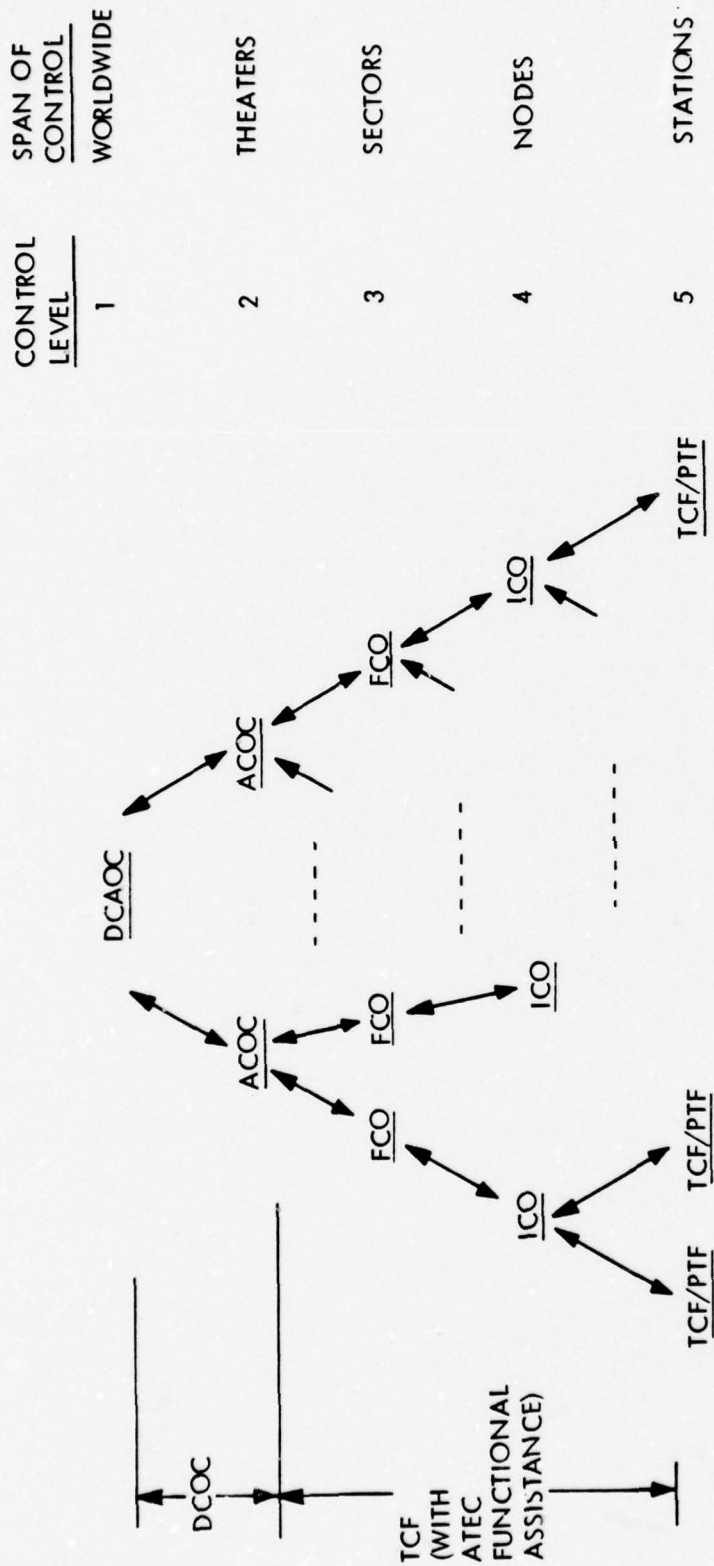




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Figure 2-6. Present SYSCON Organization





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Figure 2-7. Planned SYSCON Organization

Control Offices) to their associated FCO having Sector-wide transmission control responsibilities. Control actions at the station level will be executed manually other than automatic control actions built into the transmission equipment. Control actions requiring trunk or channel rerouting/reassignment are to be executed (operator patching actions) at WB manual patch bays that allow access to trunk signals and at Equal Level manual patch bays that allow access to the channels.

### SECTION 3

#### DIGITAL NETWORK CONTROL REQUIREMENTS AND BENEFITS

During the 1960's a number of studies [e.g., References 3-1 and 3-2] were undertaken to characterize and quantify known deficiencies in the operations of DCS technical control facilities. The output of these studies was a recommendation for automation of various technical control functions such as performance assessment, reporting, trending and fault detection/isolation and for increased standardization and modularity. Subsequent programs were initiated in order to determine cost-effective applications of automation and to develop and test related hardware and software [References 3-3 and 3-4]. The present ATEC equipment and concepts are outgrowths of these earlier programs.

The studies and programs discussed above were exercised in a DCS environment which was primarily analog (analog transmission, multiplexing, and switching) and in which control techniques were just starting to realize the benefits of modern LSI technology. As a result, many on-going programs in the area of technical control and the related system control areas of traffic control and network control are examining the impact of the present hybrid DCS, the future all-digital DCS, microelectronics and distributed processing architectures as they relate to DCS functional requirements. Examples of this are the CPMAS Program (Project 2155 Phase 2) which will integrate wideband digital facilities into the current ATEC Program, and the Modular System Control Architecture Study which will define and implement for feasibility testing modular microprocessor building blocks that realize the performance and operational requirements of system control.

Within this framework, the DNC Study will assess the functional capabilities of DCS system control to determine whether existing and proposed control techniques are adequate in an evolving DCS and to quantify, where necessary, the most effective means of improving performance.

The approach to be taken to determine the requirements and system control applications of DNC is a two-step process. First, the planned system control subsystem for the post-1970 time frame (baseline system), as described in Section 2, is analyzed in order to identify DCS performance and operational deficiencies which adversely affect service. In the present context, deficiencies refer to the non-satisfaction of requirements or the inefficient use of hardware or transmission capacity. This step entails examining both the manual and automated capabilities of system control and correlating these to performance requirements. This evaluation will reflect consideration

for programs which exist or are under development such as the AUTOVON Traffic Data Collection System and ATEC, and is designed to achieve the overall goal of increasing the operational effectiveness of the DCS.

The next step involves the evaluation of those system control areas for which deficiencies are defined. A comparative analysis is performed in order to determine the optimal application of DNC; the alternatives specifically considered include a manual implementation in the form of multiplexers and patch panels and an automatic DNC implementation in the form of a remotely controllable channel reassignment capability. The comparison will consider DCS performance benefits derived from both approaches with respect to network flexibility, availability and survivability; transmission capacity utilization; the potential for decreased manpower and operations and maintenance costs; and interoperability with the TRI-TAC network.

### 3.1 SYSTEM CONTROL CAPABILITIES

The planned system control structure for the post-1980 time frame is shown in Figure 3-1. For convenience of presentation, the three areas of system control - network control, traffic control, and transmission control - are illustrated as physically and functionally separate; however, many of the facilities employed in the three areas are, in fact, physically integrated. The concept of operations for this system control subsystem is one of adaptive control; that is, near real-time status information and exception reporting flow upward in the hierarchy in order to maintain a continual awareness of the effects of control actions. Control actions are to be applied at the lowest practical hierarchical level and should be automated where it is cost-effective to do so. This approach minimizes system control overhead, provides a large degree of manual backup, and increases network survivability.

Some of the key qualitative objectives established for the system control subsystem [Reference 3-5] which provide a guideline for the present analysis are:

- a. To provide for timely fault detection, isolation, and restoration
- b. To provide the capability for remoting sensing of information and for remoting the control of equipment
- c. To provide for automatic assessment and control of system performance whenever possible
- d. To exercise control at the lowest practical level
- e. To provide a capability for manual override of automatic control features



# HIERARCHICAL LEVEL

WORLDWIDE

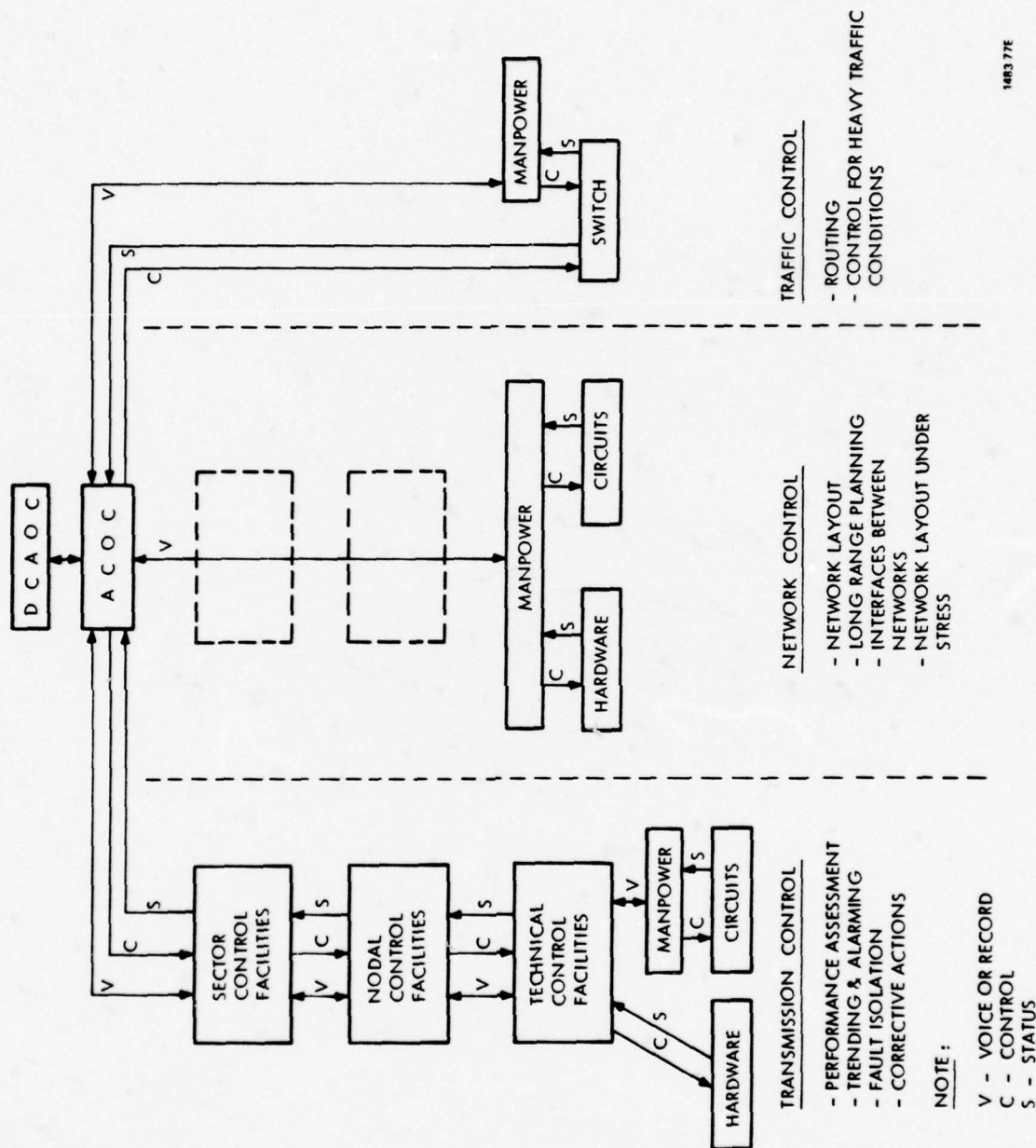
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THEATER

SECTOR

NODE

STATION



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Figure 3-1. System Control as Presently Planned

- f. To ensure that individual control elements are capable of independent operation under crisis
- g. To provide the capability to conduct subscriber-to-subscriber and local loop performance quality checks
- h. To minimize both the skill level and the number of O&M/Technical Control Personnel required to operate and maintain the DCS.

The control capabilities of the hierarchical levels are dependent upon the degree of automation and upgrading that is implemented. The DOCC elements, DCAOC and ACOC, presently have computer based systems assisting in the performance of their system control functions. The DCAOC is primarily responsible for system management functions such as logistics planning, contingency planning and allocation of physical, fiscal and manpower resources. The ACOC is responsible for coordinating lower hierarchical levels within its theater for traffic and network control analysis, and for control action initiation. With respect to traffic control, the ACOC employs computer based systems to aid in this task. For example, the AUTOVON Traffic Data Collection System and the AUTOVON Centralized Alarm System provide the capability to collect and process measurements pertaining to switch and link traffic status, to display the status of switch components, and to display alarms pertaining to special controls such as line load controls and routing table updates. With respect to network control, the control responses of the ACOC for performing network layout, long-range planning, interfaces between networks, and network responses to stress are almost entirely manual. However, computer assistance is available for the processing of raw data and as a development and planning tool.

The functional requirements established for the automation of the three lowest system control hierarchical levels have been specified [References 3-6 and 3-7]. It is expected that the ATEC program will provide the facilities for satisfying these functional requirements with an interim operational capability scheduled for early in the 1980's. The functions allocated to the planned sector, nodal and station control levels are presently performed by TCF reporting stations and their associated reported-on TCF and PTF stations. The TCFs and subordinate TCFs/PTFs are manually operated by O&M and controller personnel of the MILDEPS. The automation that will be realized at the sector, nodal and station levels is primarily in the transmission control area and is illustrated in Figure 3-2. The automation scheduled for the network control area is with respect to the data base required to perform all system control functions. The data base will provide information pertaining to the configuration and status of links, routes, trunks, nominal VF channels, telegraph/data channels, circuits and ATEC equipment.

The sector, nodal and station control interoperability requirements are defined in the ATEC System Description

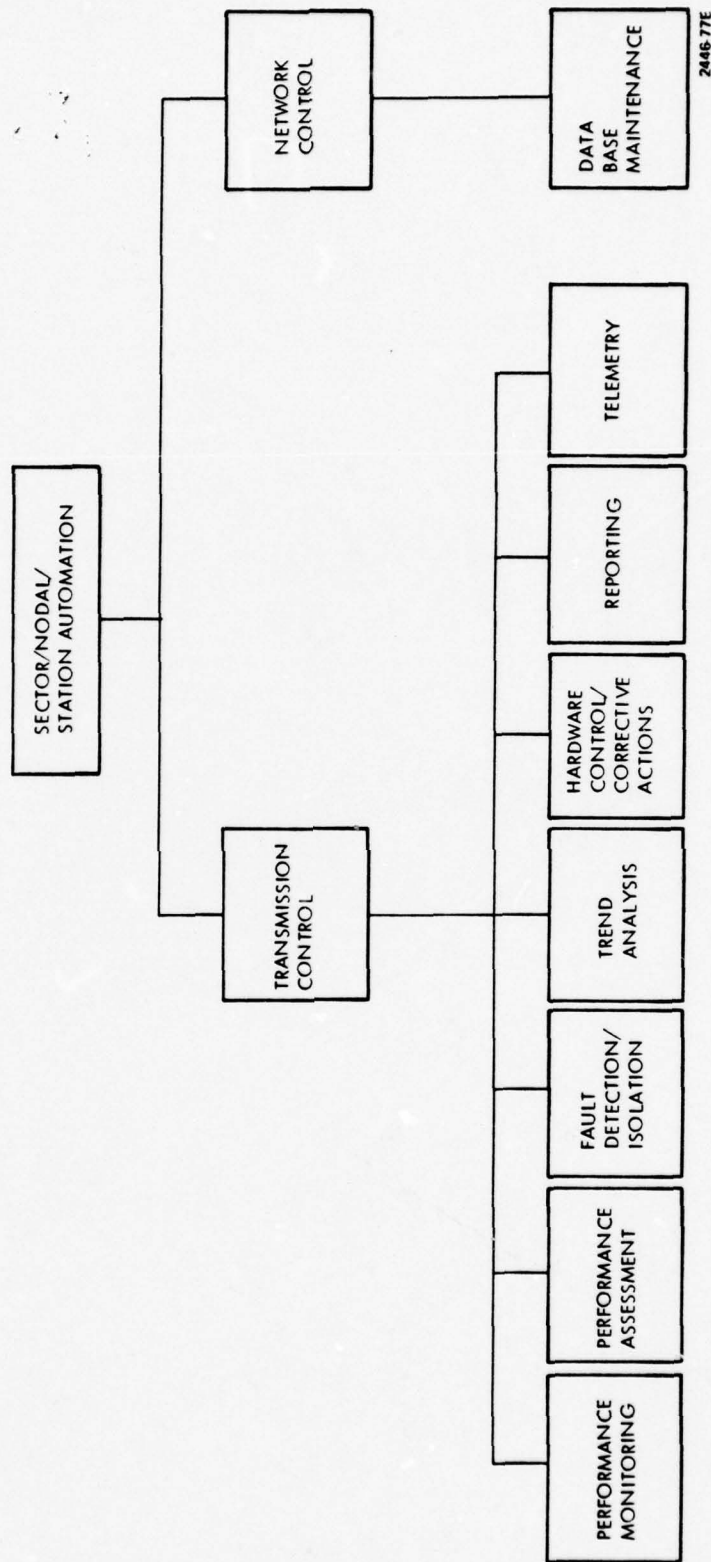


Figure 3-2. System Control Areas Affected By Sector/Nodal/Station Automation



[Reference 3-7] and summarized in Figure 3-3. As shown in this figure, direction, coordination and communication interfacing are to be performed at the higher hierarchical levels and control action execution at the lowest level. The specific sector/nodal control interoperability requirements pertinent to DNC are:

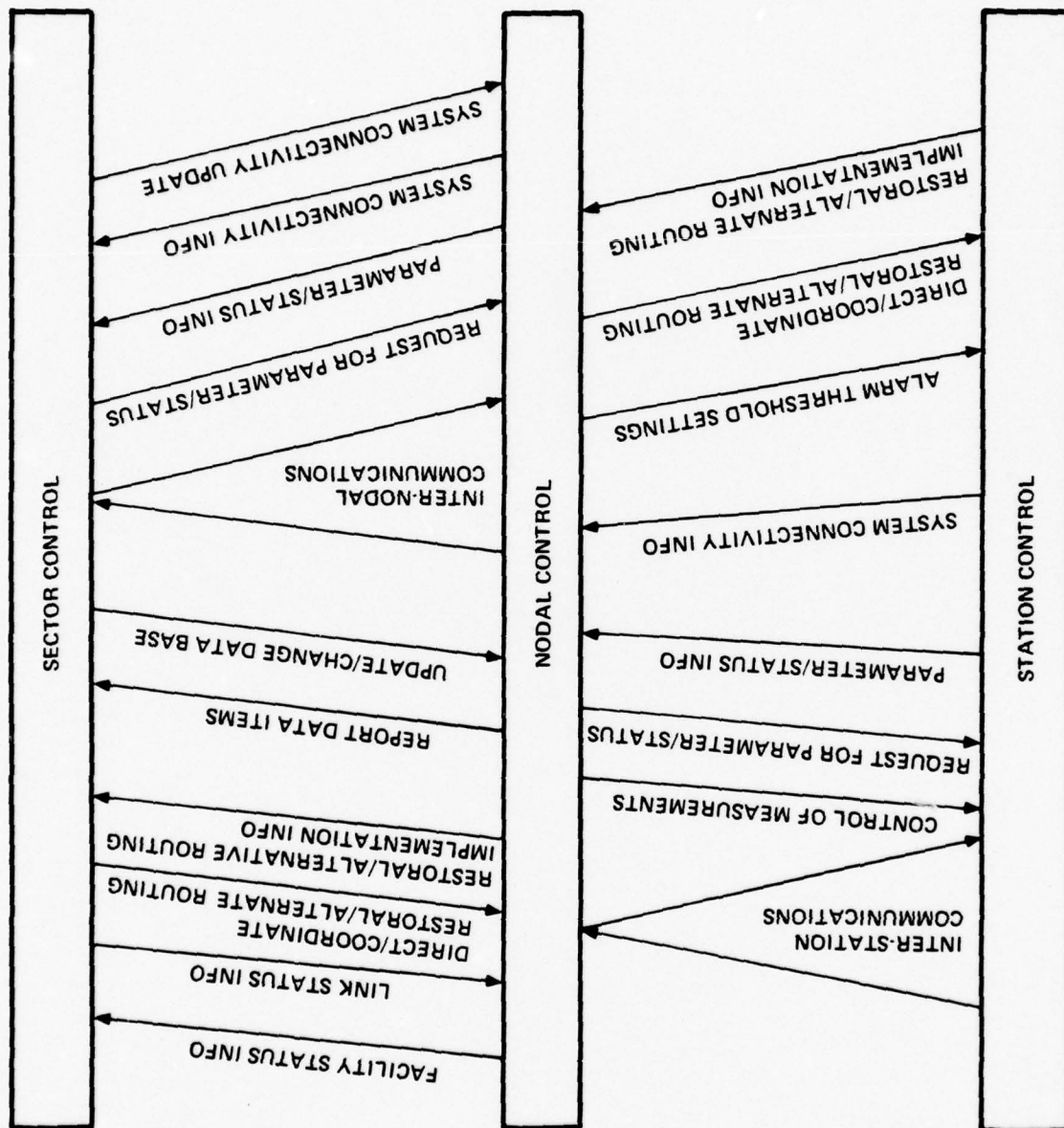
- a. Sector control will transmit restoral and alternate routing plans to nodal control. The sector will coordinate information received from nodal control regarding implementation of restoral and alternate routing.
- b. Sector control will maintain and display the complete system connectivity information for the entire theater. Nodal control shall provide connectivity information and sector control shall issue a data base update message to nodal control.
- c. Sector control shall possess an automated capability to update/change the data base of all subordinate nodal controls.
- d. Sector control shall provide the communication interface between nodal controls within a sector by monitoring and coordinating the interchange of messages between nodal controls.

The pertinent nodal/station control interoperability requirements are:

- a. Nodal control will have the capability to transmit control actions to station level technical controllers based upon restoral and alternate route plans and hardware and circuit status information. Nodal control will be notified of the results of station level actions.
- b. Nodal control will maintain the data base of all subordinate stations.
- c. Nodal control will possess the capability to coordinate status information received from sector control with status information pertaining to DCS facilities located within the nodal control's jurisdiction.

In addition to the above interoperability requirements, a stand-alone capability must exist whereby each level is capable of operating without the next higher level. It is considered operationally acceptable to fall back into a degraded mode of operation when the next higher level is inoperative. If nodal control is inoperative, the station level equipment must be able to stand alone using I/O control devices.





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Figure 3-3. Sector/Nodal/Station Interoperability

### 3.2 SYSTEM CONTROL ISSUES

Based on the capabilities of the planned system control subsystem, as described in Section 3.1, control deficiencies are identified in the transmission and network control areas. These deficiencies principally result from the lack of direct control over DCS hardware and circuits.

The upgrades planned for the five hierarchical levels will result in a high level of automation for the following network and transmission control functions:

- a. Acquisition of circuit, hardware and user status information
- b. Analysis and reduction of this data at the various hierarchical levels
- c. Dissemination of control action information.

However, almost all control action execution is based on man as a key control element. This is especially true with respect to network control where all control over circuits and hardware requires manual intervention. Although manual control per se is not detrimental, associated with it is a lack of adequate hardware to provide for flexible control of the DCS. This lack of hardware results in excessive O&M costs and inefficient use of manpower and equipment. The following subsections examine in detail the deficiencies inherent in the planned system control subsystem. Section 3.3 defines DNC requirements based on the objective of minimizing these deficiencies to the maximum extent possible and determines through a comparative analysis whether a manual or automated DNC capability is preferred.

#### 3.2.1 Transmission Capacity Utilization

Because of the limited availability of direct circuits and the complex system management required to constantly rearrange circuits, backhauling is a serious problem in all large scale networks and is a major cause of inefficient use of transmission capacity. Backhauling refers to the necessary extension of a circuit out of a site and then back to the site in order to access a desired transmission cross section.

Figure 3-4 illustrates two examples of backhauling. The first occurs in establishing a 64 kb/s circuit between users A and A' (denoted circuit A-A' in Figure 3-4). Because there is neither a direct digital group between sites 1 and 4, nor a thru-channel patching capability at site 2, it is necessary to backhaul circuit A-A' from site 2 to site 3. This backhauling results in the inefficient use of 128 kb/s of transmission capacity in the link between sites 2 and 3. Additionally, the backhauling results in

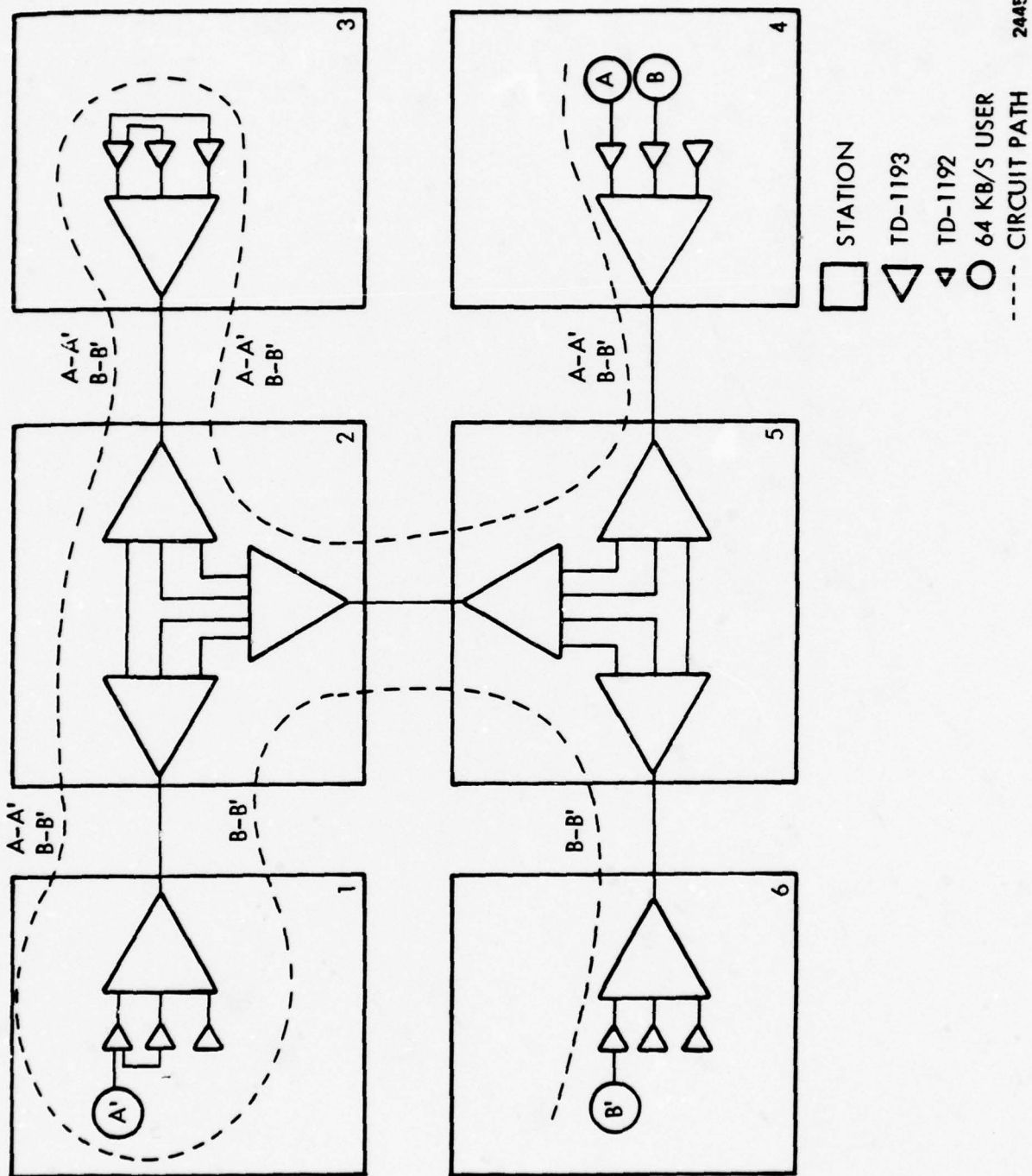


Figure 3-4. Backhauling Illustration

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decreased survivability and availability and increased O&M costs since it introduces superfluous equipment, channel miles and sites over what is required for a direct connection.

The other example of backhauling in Figure 3-4 occurs in circuit B-B' which is established between sites 6 and 4. In this case, it is assumed that there is a direct digital group between sites 6 and 4 but that it already has a full complement of 24 channels. Thus, in order to complete circuit B-B', it is necessary to backhaul from site 5 to site 2, from site 2 to site 3, and finally from site 2 to site 1. Because there is no channel breakout at site 5 in the appropriate digital groups, the required backhauling has resulted in the inefficient use of 128 kb/s of transmission capacity in each of three links. For DRAMA equipment, such utilization of 128 kb/s of transmission capacity translates into a cross-sectional inefficiency of between 1/2 and 4 percent, depending upon the size of the cross section. As in the first example, associated with this backhauling is a loss of survivability and availability and an increase in O&M cost over the same circuit routed directly.

The two backhauling examples in Figure 3-4 illustrate the two primary causes of backhauling. The first is due to a lack of a direct route which would be typical in the early stages of network development but would also be a common occurrence in mature networks. The second problem, a full direct route, is a very serious problem in developed networks, and is to be expected as the digital DCS matures. It should be noted that backhauling, because of its inherent inefficiency, is self-generating; that is, backhauling circuits eliminates capacity, thus causing other circuits to be backhauled. Unless guarded against or limited in network practices, backhauling results in a very complicated circuit structure and an equally complicated circuit management function.

### 3.2.2 Network Reconfiguration

Circuit, group and supergroup reconfigurations due to either changing requirements or stress conditions are usually complicated and time consuming to plan and implement. This is due to a general lack of spare or preemptable routes, the excessive amount of intersite coordination required, circuit interface/compatibility problems, and various system management problems related to circuit rerouting, activation and deactivation.

The major requirement in this area relates to the need to improve service restoral capabilities with respect to natural or man-made stresses. Restoration can be accomplished by routing over a spare or preemptable channel or patching in spare equipment. The operations involved in restoring service are: locating candidate reroute paths, checking compatibility and precedence (if preemption is involved), and coordinating the implementation of the reroute with other TCFs. The restoral process is extremely time consuming and because of the general lack of spare channels, few circuits are restored by rerouting. In fact, it is estimated [References 3-8 and



3-9] that less than ten percent of all failed circuits are restored by rerouting, and that the average outage time, excluding those over 4 hours, is greater than 45 minutes. Although these numbers are based on the present analog DCS, the restoration capabilities of the planned DCS, with respect to the above mentioned problem areas, should not change appreciably since the various system control upgrades are not directly addressing these problem areas.

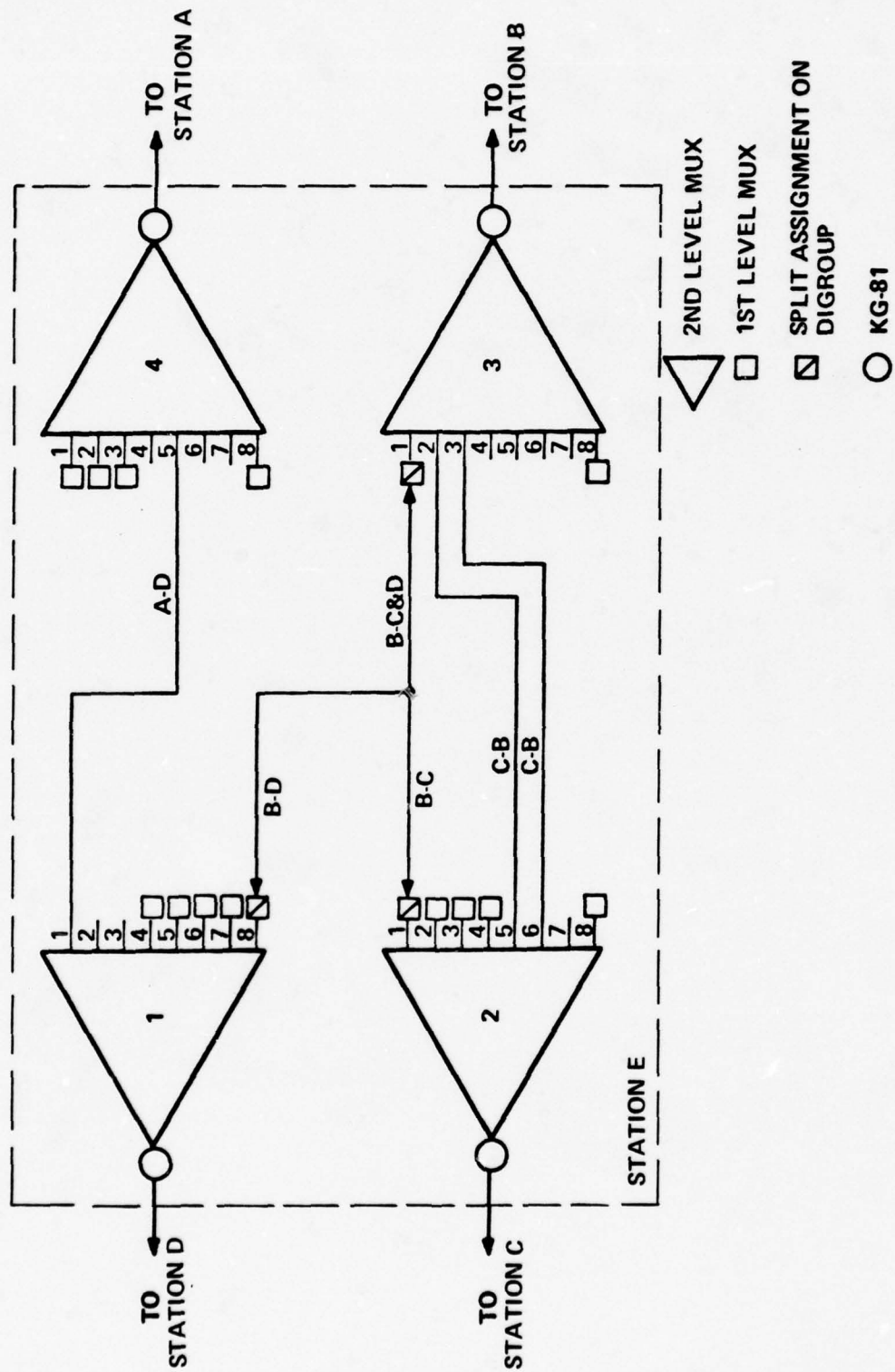
An additional aspect of the network reconfiguration problem area is the inefficient utilization of manpower required in order for system control to be able to rapidly respond to major stress conditions. Several studies [References 3-8 through 3-13] have investigated the technical controller action profile, that is, the technical controller workload by active and idle time. The results from Reference 3-9 are illustrated in Table 3-1. Because of the similarity between the data in this table and information in the other references cited, the data is assumed to be statistically reliable and to be representative of most TCFs. The eight technical controller activities listed are those activities required to perform the vast majority of technical control functions. The high proportion of idle time, shown in Table 3-1 (approximately 50 percent), is required in order that the technical controllers can rapidly respond to stress conditions requiring an inordinate amount of their time. As before, the numbers in Table 3-1 are based on the analog DCS. However, since the additional capabilities resulting from ATEC will not significantly affect the causes of the large idle time requirement, it is likely that an appreciable quantity of idle time will be required by technical controllers in the digital DCS.

### 3.2.3 Network Flexibility

Inherent in the transition to a digital DCS is a loss of network flexibility. This loss is due to a doubling of the basic transmission cross section in the digital upgrades. The analog cross section is based on the FDM group which consists of 12 channels; whereas the digital cross section is based on the TDM group which consists of 24 channels. During the early stages of digitalization, the larger cross section results in numerous unused channels while as the network matures, backhauling (as described in Section 3.2.1) becomes a problem. Also, the larger digital cross section may require additional channel breakouts along a route in order to satisfy small cross-sectional requirements. Typical of the loss of network flexibility due to digitalization is the need to perform rechannelization. Figure 3-5 illustrates the concept of rechannelization. In this example, 12 VF circuits are required between stations D and E, D and B, C and E, and C and B. As shown in this figure, three first-level multiplexers are required in order to establish the circuits for the given station multiplexer arrangement. Such a configuration of split-assigned multiplexers is inefficient with respect to equipment utilization since three first-level multiplexers are being used to drop 24 circuits, which is the capacity of a single first-level multiplexer. Based on an analysis of DEB

TABLE 3-1. TCF CONTROLLER ACTION PROFILE

ACTIVITY	CONTROLLERS		SUPERVISOR	
	AVE. DAILY TIME (MIN.)	% OF TOTAL	AVE. DAILY TIME (MIN.)	% OF TOTAL
Idle	699	48.5	792	55
Coordination	232	16	219	15
Testing	220	15	50	3.5
Patching	24	2	7	0.5
Reporting	122	9	161	11.5
Instruction	33	2	75	5
Other	102	7	136	9.5
Waiting	8	0.5	-	-



8361.79E

Figure 3-5. Example of Rechannelization



stages 2 through 4 and assuming a 50/50 split assignment for all rechannelization multiplexers, it was determined that approximately fifty first-level multiplexers are being inefficiently used for rechannelization.

#### 3.2.4 AUTOSEVOCOM II and TRI-TAC Interfaces

As presently planned, the interface between AUTOSEVOCOM II (AII) and the DCS transmission backbone and between TRI-TAC and AII (via the DCS transmission backbone) will be at the channel level. Figure 2-5 illustrates the planned AII configuration, TRI-TAC interoperability, and the major AII system components. The necessity of interfacing at the channel level is brought about by the technical control requirements of performance assessment, fault isolation and detection, and restoration.

Figure 3-6 illustrates the planned interface between AII and the transmission backbone. As shown in this figure, channel breakout of digital groups from the AN/TTC-39 (or other AII elements such as the DAX or CNCE) is provided by the DGM family of multiplexers. It is advantageous to use the DGM family for this purpose since it permits the AN/TTC-39 to transmit combined digital groups (Type 3 and 4 digital groups per ICD-003, [Reference 3-14]) to the TCF, thereby saving facilities (e.g., access lines and modems). After appearances at patch panels, the channels are multiplexed to the 64 kb/s or 128 kb/s levels using non-DRAMA submultiplexers or to the 256 kb/s or 512 kb/s levels using DGM multiplexers, buffered to absorb timing differences, and finally inputted into the first-level multiplexers.

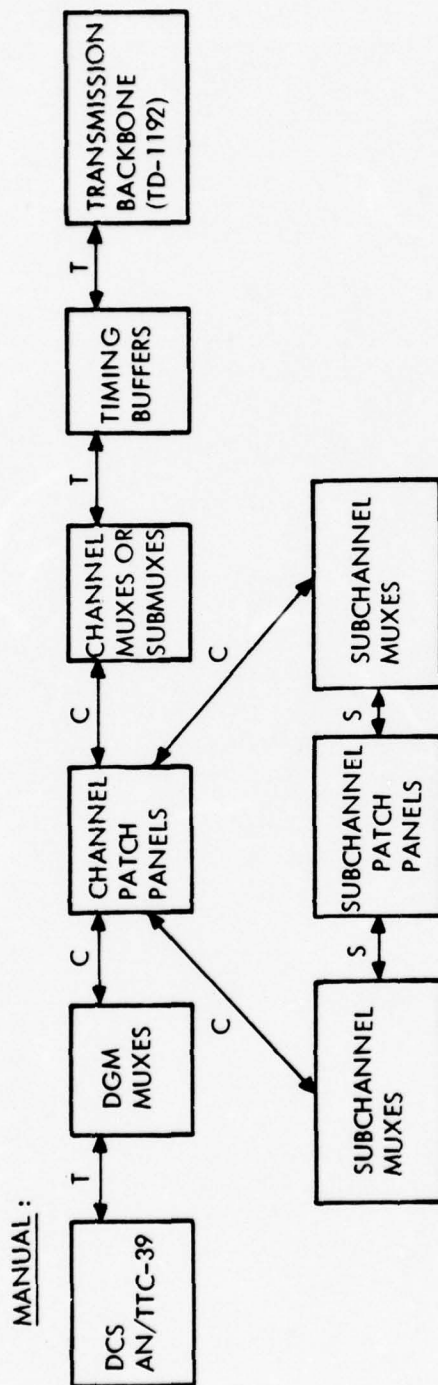
In addition to the back-to-back multiplexers required for channel breakout, back-to-back multiplexers, as shown in Figure 3-6, are required for subchannel breakout. Access to the subchannels is necessary for two reasons: first, to perform the technical control functions of performance assessment and fault detection and isolation; second, to assess the system control information contained within the AII digital group overhead channels and to provide for the transmission of this information to the ACOC and other system control levels. System control information flowing from the AII switching elements pertain to traffic status, equipment status and alarms; whereas traffic flowing to the switching elements would pertain to traffic controls which are to be applied.

The AII/TRI-TAC/DCS transmission backbone interoperability, as described above, limits network flexibility and efficiency with respect to the following:

- a. An interface based upon the use of back-to-back multiplexers for channel and subchannel breakout is complex to implement and maintain, and expensive and unreliable compared to solid state functional modules with built-in test and diagnostic capabilities.



# AUTOSEVOCOM II INTERFACE WITH THE TRANSMISSION BACKBONE



## MANUAL APPROACH

- REQUIRES BACK-TO-BACK MULTIPLEXERS FOR CHANNEL BREAKOUT TO PERFORM TECHNICAL CONTROL ACTIVITIES
- RESULTS IN INEFFICIENT USE OF TRANSMISSION CAPACITY (OVERHEAD AS HIGH AS 25 PERCENT)
- REQUIRES BACK-TO-BACK SUBCHANNEL MULTIPLEXERS TO ACCESS AN/TTC-39 SYSCON SUBCHANNELS

## NOTE :

- S SUBCHANNELS
- C CHANNELS
- T TRUNK GROUPS

1462 77E

Figure 3-6. Digital Network Control Requirement

Additionally, this manual interface, based on mechanical-contact patch elements, requires routine or scheduled maintenance since the patch elements are subject to environmental wear.

- b. The channel submultiplexers inefficiently utilize transmission capacity with overhead as high as 25 percent. This is due to the fact that framing for the submultiplexers displaces a single 16 kb/s channel.
- c. TRI-TAC interfacing is limited to DCS stations which have first-level multiplexers.
- d. The maximum AII digital group rate, which is compatible with the first-level multiplexer, is 512 kb/s. This limits the cross-sectional growth of AII interswitch trunk groups to well below the capabilities of the AN/TTC-39.

Another issue to be considered is that TRI-TAC must be able to use the DCS as simply a transparent media, that is, enter at one DCS station and exit at another. Since the framing pattern format and frequency (a 1010--- pattern with 4 kHz repetition rate) of TRI-TAC digital groups at the 32 kb/s digitalization rate is identical to the T1 framing pattern format and frequency, it is not possible to directly input TRI-TAC trunk groups into the first-level multiplexer. Thus, a special interface device capable of altering the framing pattern format within TRI-TAC digital groups would have to be devised or the interface would have to be limited to individual voice channels, data channels, and overhead channels with the framing subchannel suppressed.

### 3.3 DIGITAL NETWORK CONTROL REQUIREMENTS

In the previous section, DCS performance and operational deficiencies inherent in the planned system control subsystem were examined and discussed. It was determined that the planned system control structure is inadequate with respect to certain circuit and hardware control capabilities in the functional areas of network and transmission control. Additionally, it was shown that the deficiencies result in reduced network flexibility and the inefficient use of manpower, equipment and circuit mileage.

Within this section, DNC requirements are developed. These requirements will provide the guidelines for subsequent investigation of DNC with respect to applications and implementation. DNC requirements are derived such that augmenting DCS system control with a DNC capability minimizes and where possible eliminates the deficiencies discussed in Section 3.2. It should be noted that DNC is designed with the overall goal of increasing the operational

effectiveness of the DCS. Those areas identified for DNC are those areas for which present manual system control performance is inadequate and for which hardware in combination with some degree of automation is not planned or ineffective in the digital DCS.

Within each of the system control problem areas examined, the capabilities of manual and automated DNC will be analyzed and compared in order to determine the optimal application of DNC. This comparative analysis will consider manual DNC implemented as patch panels and multiplexers (where necessary) and automated DNC implemented as remotely controllable channel reassignment hardware. The former would utilize existing manual control techniques and apply them within the DCS where necessary to realize DNC functions. The latter would employ control techniques which realized the DCA qualitative objectives established for the future DCS, as discussed in Section 3.1.

For clarity of presentation, the following subsections are organized so that they parallel the discussion of the various system control issues of Section 3.2. This provides a simple means for correlating problem areas with DNC requirements and applications. Section 3.4 describes DCS performance benefits which derive from the required DNC capabilities established in this section.

#### 3.3.1 Transmission Capacity Utilization

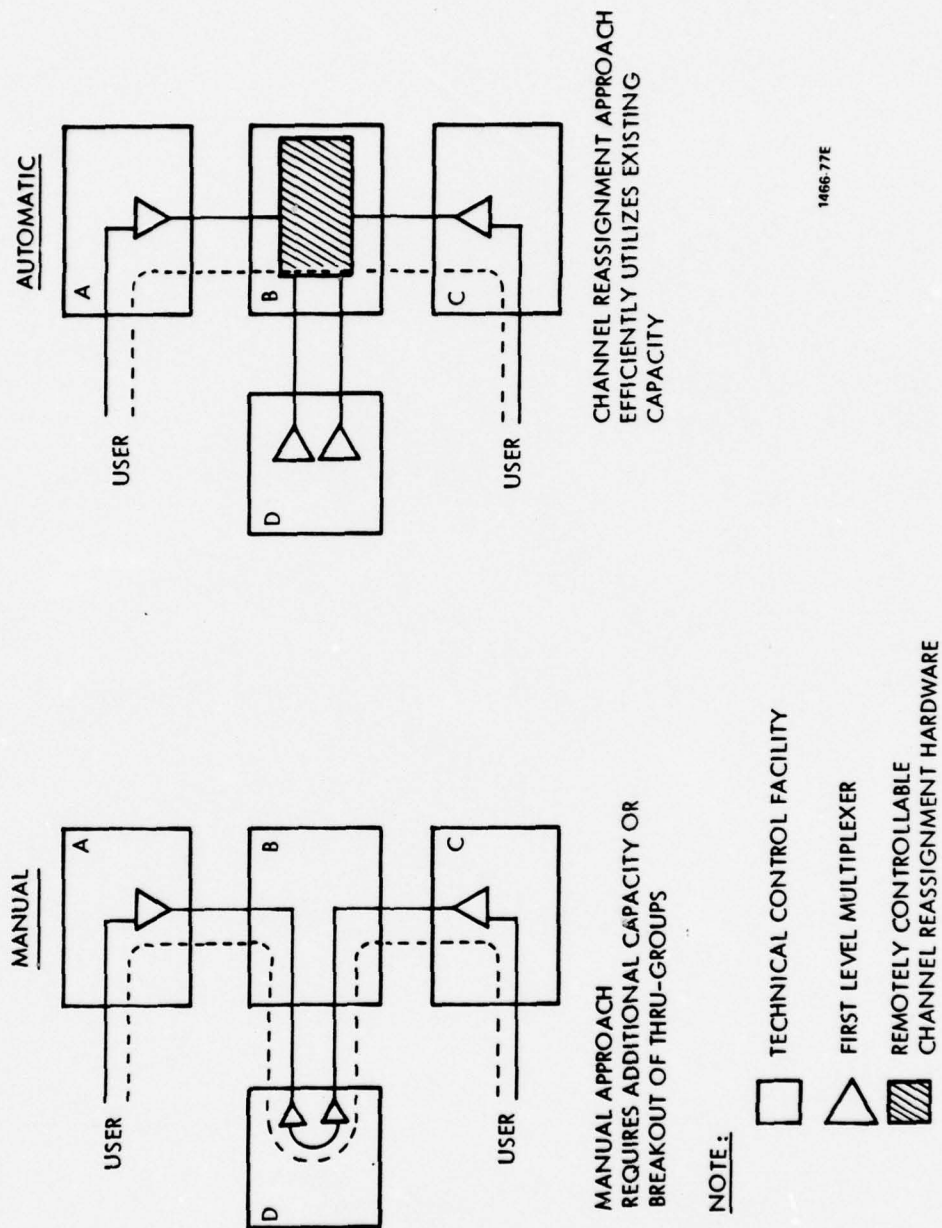
As discussed in Section 3.2.1, backhauling of circuits is a major cause of inefficient use of transmission capacity. DNC, through a channel reassignment approach, is capable of significantly increasing transmission capacity utilization by eliminating backhauling. It does this by providing the capability to reassign channels between thru-groups, thus obviating the need to backhaul. The channel reassignment capability must be applicable to 64 kb/s PCM byte-oriented channels used in T1 digital groups, 16/32 kb/s bit-oriented channels used in TRI-TAC formatted digital groups, and 2/4 kb/s bit-oriented subchannels which make up the TRI-TAC overhead channels.

Figure 3-7 illustrates the manner in which both automated and manual DNC would be applied to eliminate backhauling. For the example of Figure 3-7, a circuit is to be established between a user connected to TCF A and a user connected to TCF C. Because there is no direct digital group between the two TCFs, it is necessary to backhaul the circuit from TCF B to TCF D. As may be seen, the manual approach offers no advantage over present control techniques since this approach requires either additional capacity in the form of another direct digital group, or channel breakout of the thru-groups involved. On the other hand, the automatic DNC approach, which provides the capability to reassign channels between any digital groups to which it is connected, eliminates the backhauling.



REQUIREMENT: EFFICIENTLY UTILIZE TRANSMISSION CAPACITY BY  
ELIMINATING BACKHAULING

APPROACHES:



1466-77E

Figure 3-7. Digital Network Control Transmission Utilization Requirement



In effect, the channel reassignment capability implements channel breakout, circuit patching, and a digital multiplex applique function without back-to-back multiplexers and patch panels. Thus, channel reassignment is functionally preferred over a manual approach since the latter would require channels to be dropped to baseband in order to realize a channel reassignment capability and therefore offers no advantage over the baseline system control subsystem.

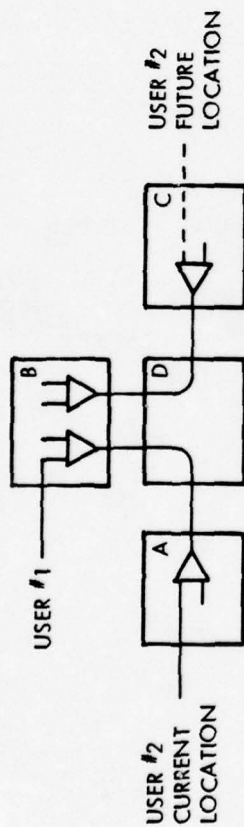
### 3.3.2 Network Reconfiguration

DNC when implemented as an automated channel reassignment capability would permit the rapid reconfiguration of the DCS from central locations by eliminating first-level multiplexer input port card incompatibility problems, increasing the availability of spare and preemptable channels, and permitting rerouting of channels in thru-groups. The latter is extremely important because when it is employed at branching stations, it can create routes which did not previously exist. DNC generates new routes in the same manner in which it eliminates backhauling; that is, it reassigns channels between thru-groups, thus creating thru-channels when there were none previously. The number of thru-channels that can be established at a station between two connected stations is limited only by the number of spare or preemptable channels in the links connecting the sites. In general, the number of circuits that can be established between any two stations in a network which employs DNC is a complicated function of the type, the quantity and the location of channel reassignment hardware deployed within the network. Section 4.3 examines in detail the issues involved in the network deployment of DNC hardware.

Not only can DNC provide for the rapid reconfiguration of channels, it can also reconfigure digital groups and supergroups. It does this by reassigning the channels and subchannels associated with the groups and supergroups to be reconfigured. When implemented as an automatic capability, DNC will perform this high level reconfiguration with essentially the same speed with which it will reassign a channel.

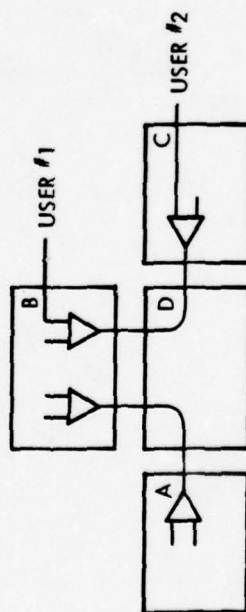
Channel reassignment also reduces, in many cases, the number of activations and deactivations associated with a reconfiguration and will permit the operation to be performed remotely from a central location such as an ATEC intermediate control office. This not only reduces manpower requirements but also significantly increases the speed with which reconfigurations can be accomplished. Figure 3-8 shows the manner in which DNC, when implemented as a channel reassignment capability, reduces activations and deactivations. In the example shown, the location of user #2 is changing such that his access line must be moved from TCF A to TCF C. Although user #1 is not changing locations, the manual approach requires a circuit deactivation and activation for user #1; whereas with the channel reassignment approach, user #1 is unaffected by the location change for user #2.

REQUIREMENT: CAPABILITY TO RAPIDLY RECONFIGURE NETWORK TO MEET USER DEMANDS AND STRESS CONDITIONS



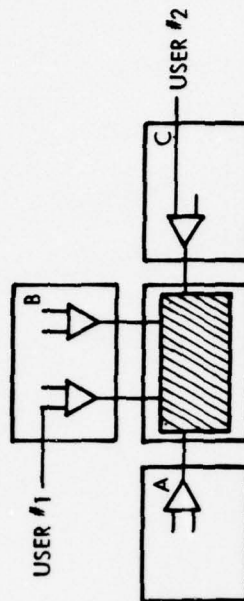
APPROACHES:

MANUAL



MANUAL APPROACH  
REQUIRES CIRCUIT DEACTIVATION AND  
ACTIVATION FOR USER #1

AUTOMATIC



CHANNEL REASSIGNMENT APPROACH  
DOES NOT REQUIRE CIRCUIT  
DEACTIVATION OR ACTIVATION FOR  
USER #1

NOTE:



TECHNICAL CONTROL FACILITY



REMOTELY CONTROLLABLE  
CHANNEL REASSIGNMENT HARDWARE



FIRST LEVEL MULTIPLEXER

1460 77E

Figure 3-8. Digital Network Control Reconfiguration Requirement

As with backhauling, manual DNC offers no advantage over present system control facilities and techniques. However, automated DNC offers a potential for rapid, flexible network reconfiguration from central locations with attendant reductions in the level and skill of technical control personnel required.

### 3.3.3 Network Flexibility

Automated DNC provides network flexibility exceeding that available in the analog hierarchy. This added flexibility derives from the channel reassignment capability which permits access to any or all channels at a TCF. In general, the channel reassignment approach requires breakout only for terminating channels and thereby eliminates having to drop all channels in a group in order to access part of the group.

As shown in Figure 3-9, manual DNC does not provide any advantage over the baseline system control subsystem, since it does not obviate the need to drop all channels to baseband. However, automated DNC permits consolidating all channels to be dropped to baseband in the minimum number of first-level multiplexers and thus realize first-level multiplexer savings. Also to be considered is the fact that a reduction in first-level multiplexers translates into a potential for reducing the number and size (input ports) of second-level multiplexers which in turn would permit a reduction in radio bandwidths. Based on an analysis of DEB stages 2 through 4 and assuming a 50/50 split assignment for all rechannelization multiplexers, it was determined that twenty first-level multiplexers could be eliminated if a channel reassignment capability is provided.

### 3.3.4 AUTOSEVOCOM II and TRI-TAC Interfacing

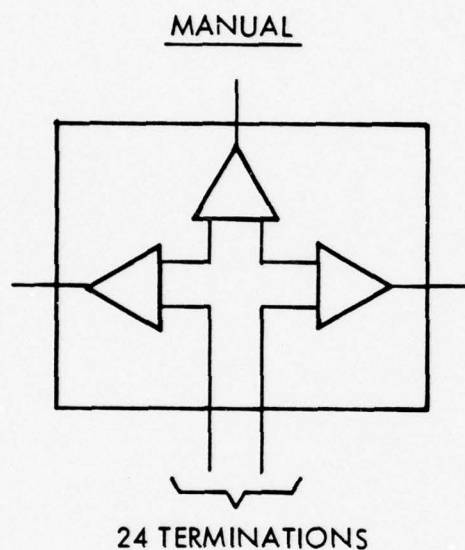
With respect to interfacing AUTOSEVOCOM II (AII) to the DCS transmission backbone and TRI-TAC to AII, automated DNC reduces the complexity of these interfaces and increases transmission capacity utilization. Manual DNC does not realize these benefits since it does not provide the equivalent capabilities with respect to digital multiplex applique and channel reassignment.

As shown in Figure 3-6, the planned interface will employ back-to-back multiplexers and patch panels. Channel reassignment hardware would eliminate this equipment and result in the simplified interface shown in Figure 3-10. The hardware would accept TRI-TAC formatted digital groups directly from the AN/TTC-39 (or any other AII equipment such as the CNCE or DGM family) and reassign its component channels and subchannels to the appropriate T1 digital groups in exactly the same manner in which it reassigns PCM channels (as described in Sections 3.2.1 through 3.2.3). Furthermore, it would provide for the breakout of those channels and subchannels required for technical control and traffic control purposes, as discussed in Section 3.2.4. Channels would be dropped on an individual basis without the need to breakout an entire group.

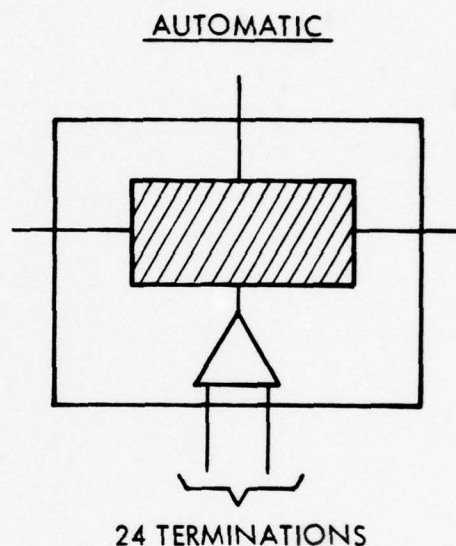


REQUIREMENT : MAINTAIN NETWORK FLEXIBILITY DURING AND AFTER THE TRANSITION TO A DIGITAL DCS

APPROACHES :



MANUAL APPROACH  
REQUIRES BREAKOUT OF  
ALL CHANNELS



CHANNEL REASSIGNMENT APPROACH  
REQUIRES BREAKOUT ONLY  
FOR TERMINATING CHANNELS

NOTE :



TECHNICAL CONTROL FACILITY



FIRST LEVEL MULTIPLEXER

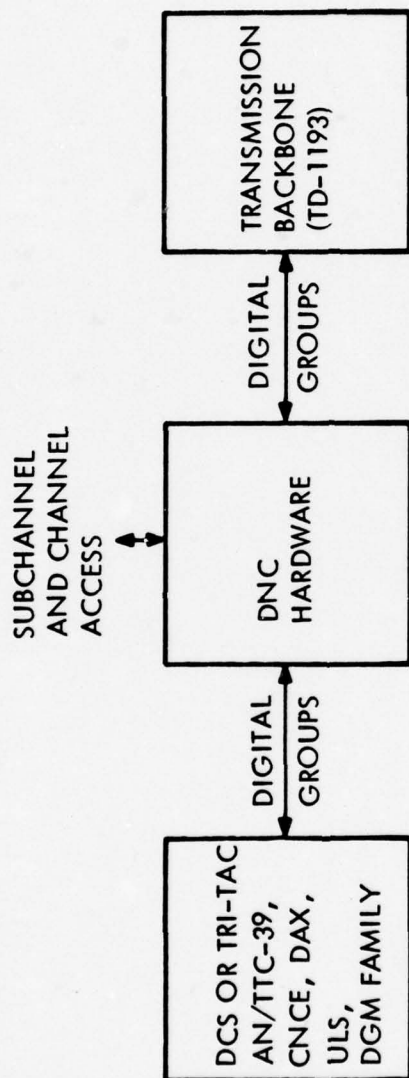


REMOTELY CONTROLLABLE  
CHANNEL REASSIGNMENT HARDWARE

1468-77E

Figure 3-9. Digital Network Control Flexibility Requirement





#### CHANNEL REASSIGNMENT APPROACH

- DOES NOT REQUIRE BACK-TO-BACK CHANNEL MULTIPLEXERS
- RESULTS IN EFFICIENT USE OF TRANSMISSION CAPACITY
- DOES NOT REQUIRE BACK-TO-BACK SUBCHANNEL MULTIPLEXERS

1470-77E

Figure 3-10. Automatic Digital Network Control Interface Requirement

The automated approach permits interfacing the AN/TTC-39 at any of its nominal trunk group rates. The proposed approach limits the maximum interswitch group rate to 512 kb/s which is the largest group rate compatible with the first-level multiplexer. However, the channel reassignment approach places no constraints on the AN/TTC-39 which could then operate at its designed modularity of from 8 to 72 channels per group (128 to 1152 kb/s).

Automated DNC also increases transmission capacity utilization by eliminating the need to rob a 16 kb/s channel for framing, as is required with submultiplexers. The channel reassignment hardware can insert four 16 kb/s TRI-TAC formatted channels into each 64 kb/s channel in a T1 digital group and maintains multiplexing integrity by using the T1 synchronization pattern in place of a separate framing pattern. Similarly, for eight 16 kb/s channels, exactly 128 kb/s (two 64 kb/s channels) of transmission capacity would be required. This efficiency is not possible in the planned interface. In a similar fashion, channel reassignment would permit TRI-TAC digital groups which are based on a 32 kb/s digitalization rate to be carried by the DCS transmission backbone without interfering with the first-level multiplexer framing, as discussed in Section 3.2.4. The channel reassignment hardware would eliminate the need for a special interface by suppressing the TRI-TAC framing (channel reassign a dummy pattern) and utilizing the T1 pattern instead.

### 3.4 SYSTEM CONTROL OPERATIONAL BENEFITS

Section 3.3 demonstrated that augmenting the planned DCS system control subsystem with automated DNC results in additional control capabilities which minimize and in many cases eliminate existing control deficiencies. Because of the importance of these capabilities, they are defined as DNC requirements. In addition to these requirements, DNC affords system control with other performance and operational benefits which are advantageous for their potential to decrease DCS O&M costs and increase network availability and survivability. These benefits are discussed below.

- a. Rapidly Restore High Priority Circuits - Through channel reassignment, DNC reduces the coordination time required to set up a restoration, increases the flexibility with which the restoration can be accomplished, and decreases the execution time required to effect the restoration. DNC reduces coordination and execution time through its remote controllability. In many cases, the restoration can be fully controlled from a central location, such as a system control nodal station, without having to involve technical controllers at stations through which the circuit passes. DNC increases flexibility by providing the capability to reroute a channel, several channels, a group or a supergroup in one operation; to reroute channels between thru-groups without channel breakout; and to eliminate first-level multiplexer input port card incompatibilities. The last capability refers

to the fact that channel reassignment reroutes information within digital groups and does not physically patch circuits.

- b. Provide Performance Assessment Tool - DNC permits the injection and extraction of test signals, the in-service monitoring of channels or groups, and the testing of channels in thru-groups where there is no channel breakout. Thus, DNC would be valuable to ATEC as a tool for accomplishing the technical control functions of performance assessment and monitoring.
- c. Provide Fault Isolation Tool - DNC can automatically loopback a channel, several channels, a group or a supergroup in either direction in one control action. In this mode of operation, DNC affords ATEC a powerful fault isolation tool. In addition, loopbacking provides a quick and accurate means for testing the transmission media, user terminals and access lines.
- d. Allow Remote Control - The automated DNC approach, in conjunction with ATEC, can remotely implement a technical control at unattended stations and provide for unattended operation at some stations which are planned for attended operation in DEB.

DNC, through channel reassignment, would enable ATEC to remotely perform the following control functions at unattended stations:

- 1. Circuit Restoration and Reconfiguration
- 2. Patching of Equipment
- 3. Monitoring
- 4. Test Signal Injection and Extraction
- 5. Reporting of Control Actions Executed.

### 3.5 SUMMARY AND CONCLUSIONS

Within Section 3, the requirements of DNC were logically developed. An evaluation of the capabilities of the planned system control subsystem revealed major control deficiencies which were used as a basis for establishing DNC requirements and its optimal application to the digital DCS.



The system control deficiencies, identified and discussed in Section 3.2, fall into four general categories of issues:

- a. Transmission Capacity Utilization
- b. Network Reconfiguration
- c. Network Flexibility
- d. AUTOSEVOCOM II and TRI-TAC Interfaces.

These four areas were then used to define identical categories of DNC operation for which requirements and applications were established in Section 3.3. Also within Section 3.3, a comparative analysis between manual and automated DNC was qualitatively performed for each category of DNC operation. Figure 3-11 shows some of the major aspects of the two approaches to DNC. In general, a manual DNC capability offers no advantage over the baseline system control subsystem; whereas an automated capability offers greatly increased network flexibility in addition to the benefits shown in Figure 3-11. Thus, automated DNC in the form of a channel reassignment capability is the preferred approach.

As discussed in Section 3.4, DNC provides system control with operational benefits other than those which are identified within Section 3.3. These benefits primarily fall into the area of transmission control and relate to the increased and automatic control capability obtained with respect to circuit routing and restoration, performance assessment, and fault isolation. Assuming these benefits define a fifth category of DNC operation, Figure 3-12 illustrates the relationship between DNC, its types of application to the DCS, and overall benefits the DCS derives from its application. Summarizing the results of Section 3.3, each of the DCS benefits gained can be conveniently grouped into one of five categories:

- a. Hardware Savings
- b. Manpower Savings
- c. Circuit Mileage Savings
- d. Increased Availability
- e. Increased Survivability.

The following sections of this report consider the application of DNC within the DCS and its optimal software and hardware implementation so as to maximize the above benefits to the DCS.

- **MANUAL**
  - **REQUIRES EXTENSIVE COORDINATION**
  - **SLOW**
  - **ERROR PRONE**
  - **EXPENSIVE - CONTINUING**
  - **INFLEXIBLE - TRAINING TIME**
  - **INEFFICIENT USE OF TRANSMISSION FACILITIES**
- **AUTOMATED**
  - **REMOTELY CONTROLLABLE FROM A CENTRAL LOCATION**
  - **DECISIONS EXECUTED RAPIDLY**
  - **AUTOMATIC ERROR DETECTION AND/OR CORRECTION**
  - **AUTOMATIC FEEDBACK OF STATUS**
  - **COMPLETELY FLEXIBLE**
  - **RELATIVELY INEXPENSIVE - ONE TIME COST**

1478.77E

Figure 3-11. Summary of Comparative Analysis Between Manual and Automated Digital Network Control

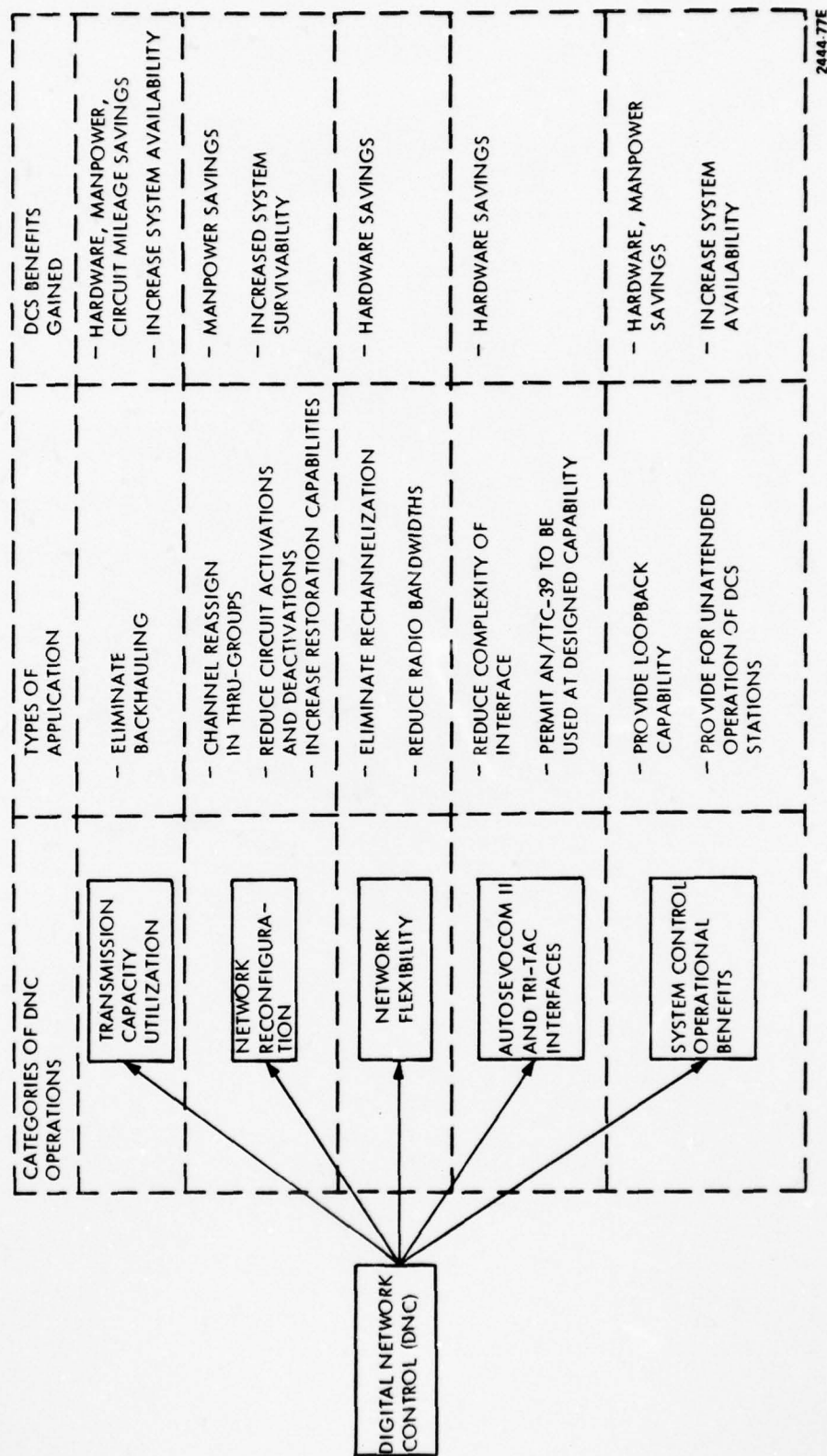


Figure 3-12. DNC Application Summary



## SECTION 4

### DIGITAL NETWORK CONTROL APPLICATION TO THE DCS

Section 3 describes the requirements for DNC in the digital DCS. This section examines how DNC should be integrated into the planned DCS in order to meet the requirements. The following aspects of DNC application are discussed:

- a. location of channel reassignment hardware within the DCS multiplex hierarchy
- b. hardware modularity with respect to size and functions
- c. network deployment of DNC hardware and its relationship to network flexibility
- d. synchronization
- e. man/machine interface
- f. availability
- g. COMSEC
- h. DNC scheduling.

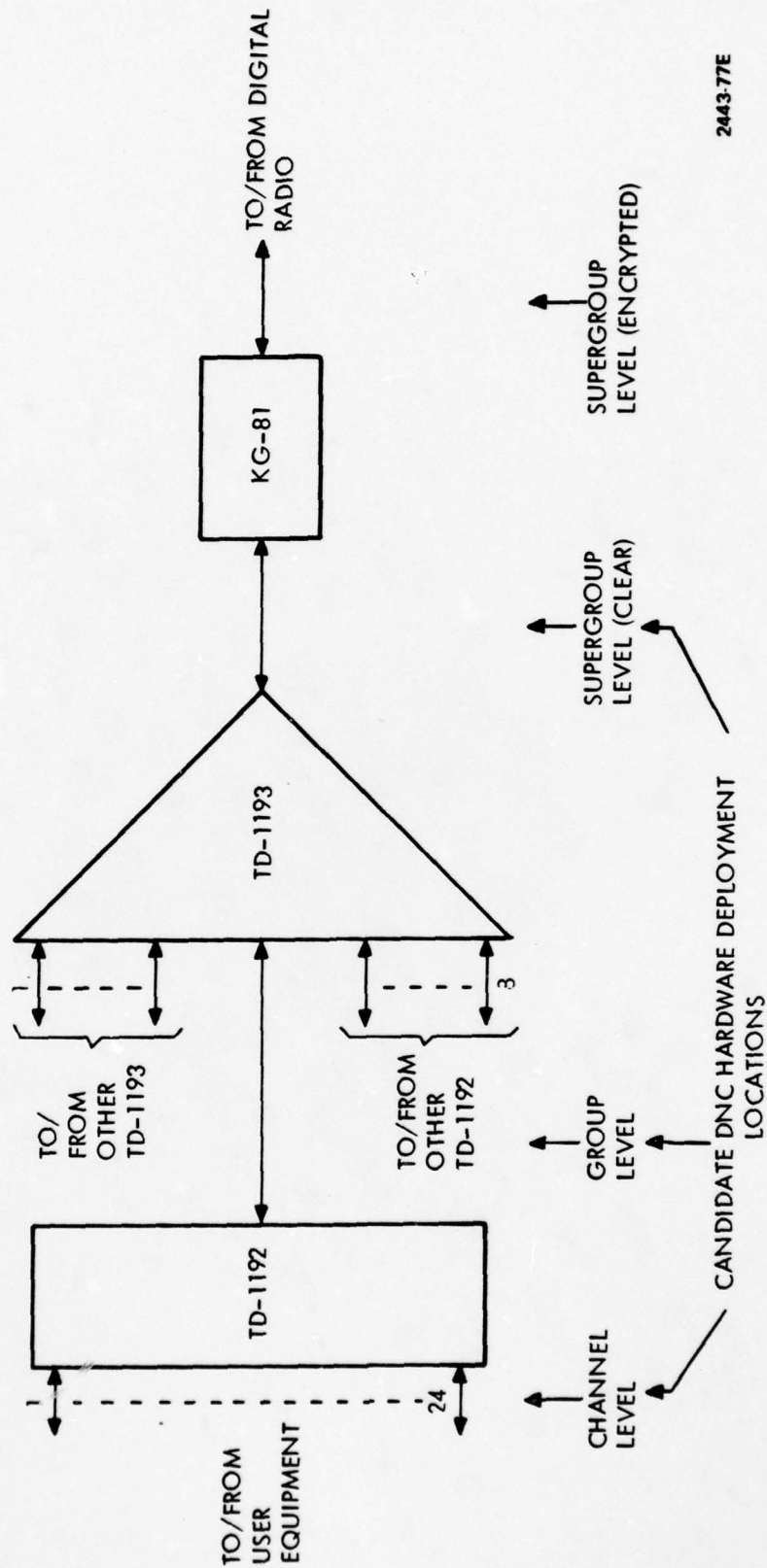
When practical, alternatives within each area of application are contrasted and compared in order to select the optimum approach for DNC and to establish baseline design requirements for its implementation. This implementation is discussed in detail in Sections 5, 6 and 7.

#### 4.1 MULTIPLEX HIERARCHY

This section determines the preferred location of DNC hardware within the planned European multiplex hierarchy. The analysis assumes utilization of DRAMA equipment and considers as deployment candidates the three hierarchical levels shown in Figure 4-1. The supergroup level at the encrypted side of the KG-81 bulk encryptor is not considered because the encryption renders channel reassignment impossible, as discussed in Section 4.7. The three levels considered are compared with respect to their ability to satisfy DNC requirements, as described in Section 3.

##### 4.1.1 Channel Level

The channel level refers to the equipment side of the TD-1192 which terminates 4 kHz analog users and a variety of digital rates and types from 0-20 kb/s asynchronous to 512 kb/s synchronous. One advantage to this level is that the CY-104s used in DEB Stage 1 can be



2443-77E

Figure 4-1. Multiplex Hierarchy

accommodated. Placing DNC hardware at a higher level precludes reassignment of channels which pass through a CY-104 because they are in an encrypted group (refer to Section 4.7).

There are three major disadvantages to implementing DNC at this level. First, in order to access channels in thru-groups, (i.e., bit streams which pass through a station without being broken out to the channel level), TD-1192s would be required. Thru-group access is an important requirement of DNC in order to eliminate backhauling and to maintain network flexibility (refer to Sections 3.2 and 3.3). Second, AUTOSEVOCOM II and TRI-TAC would be limited to rates compatible with the TD-1192, as in a manual implementation, because the interface to the transmission backbone is at the channel level. Third, many TD-1192 inputs are port card incompatible, such as analog and digital inputs or digital inputs of different rates and/or modes of synchronization. This would limit the reassignment capability needed to perform DNC functions because all channels are not compatible with all other channels.

#### 4.1.2 Group Level

The group level refers to 1.544 Mb/s T1 format digital groups which connect to the line side of the TD-1192 or the equipment side of the TD-1193. The three disadvantages of the channel level approach (refer to Section 4.1.1) are eliminated here. Access to channels in thru-groups is direct because thru-groups are at the group level. AUTOSEVOCOM II and TRI-TAC are not limited to rates compatible with the TD-1192 because channel reassignment at the group level can provide a Digital Multiplex Applique function, inserting TRI-TAC formatted digital groups into the T1 digital groups. Also, there are no incompatibility problems because everything appears as one or more 64 kb/s channels at the group level and, although two incompatible devices cannot be directly connected together, a channel previously used by a teletype can be preempted in order to reroute a voice user over that channel. This cannot be done at the channel level without manually changing cards in the TD-1192.

There are two drawbacks to implementing DNC at the group level. First, channels which enter the DCS via a CY-104 cannot be reassigned, as mentioned previously. Second, some thru-groups pass through stations at the supergroup level, such as at Wurzburg in DEB IV. TD-1193s would be required to break the supergroup down to the group level if DNC hardware is required at this location.

#### 4.1.3 Supergroup Level

The supergroup level consists of those rates which interface the line side of the TD-1193 and the clear side of the KG-81. These rates are 3.168, 6.336, 9.504 and 12.672 Mb/s. An advantage of this level is that thru-groups at the supergroup level can be accommodated directly, instead of requiring additional multiplexers as would implementation at the group level. The three advantages of this group level over the channel level are also present at this level.



There are several disadvantages at this level. As at the group level, channels which pass through CY-104s cannot be reassigned. There are four different bit rates which must be handled at the supergroup level, as opposed to only one rate at the group level. The format is more complicated than the T1 format due to bit stuffing. Also, synchronization and alignment must still be provided for the groups within the supergroups in order to determine the location of individual channels in the bit stream. Finally, the higher data rates, particularly the 12.672 Mb/s rate, may pose problems in the hardware implementation and increase costs.

#### 4.1.4 Selected Level

The group level is the level chosen for deployment of DNC hardware. The channel level is unacceptable because of its inability to access thru-groups without the addition of TD-1192s and because of channel incompatibility problems. The supergroup level is unacceptable because of the more complex frame structure, multiple rates, and the fact that groups still must be synchronized in order to reassign channels within the supergroup. The drawback to the group level, that thru-supergroups must be broken out in order to reassign channels in them, is not a serious consideration because it is a rare occurrence in the planned digital European DCS.

#### 4.2 MODULARITY

In order to provide a cost-effective implementation of Digital Network Control, the hardware must be modular in both size and functions. In other words, the hardware must be configurable to the requirements of a station in the DCS at a given point in time. As the requirements of the station change, the DNC hardware must be reconfigurable in order to continue meeting the stations' requirements in a cost-effective manner.

Obviously there is a trade-off involved in modularity. A high degree of modularity results in an increased cost for a given configuration because of the hardware necessary to support the modularity, such as more cards, connectors, wiring, and so on. Also, additional O&M manpower is required because there is more hardware to reconfigure (i.e., more hardware is capable of being reconfigured than with a low level of modularity) and because reconfiguration occurs more often (i.e., the hardware tracks the requirements more closely). A low level of modularity results in more stations having underutilized hardware. These two factors, increased cost and underutilization, must be weighed against one another in order to arrive at a cost-effective solution. This question cannot be fully answered until more is known about the design of the hardware, as discussed in Sections 6 and 7. However, the following subsections describe the two types of modularity required and present implementation decisions and guidelines.

#### 4.2.1 Function

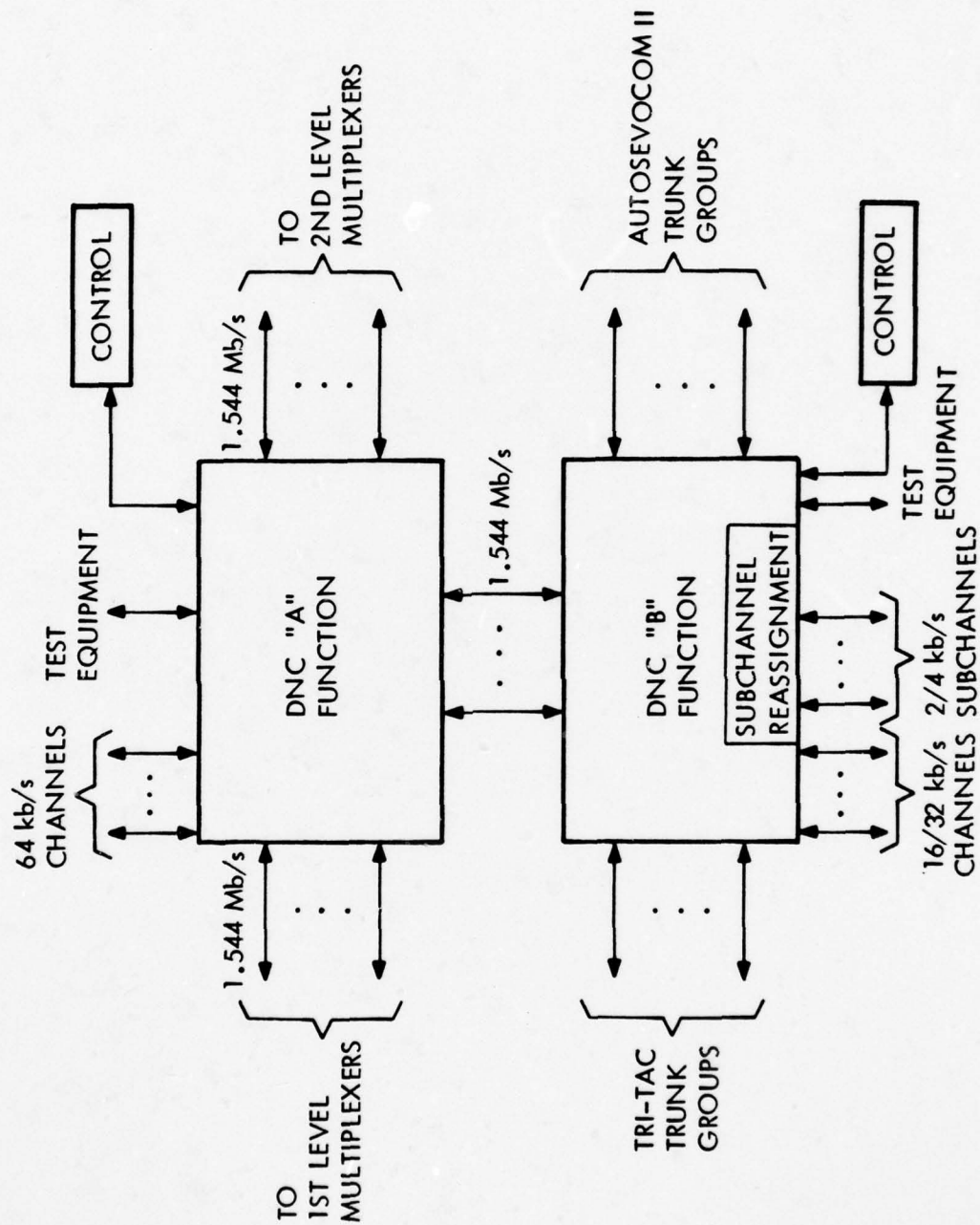
Functional modularity refers to the capability of the hardware to be configurable to the functional requirements of a station. There are four functional divisions which can be made for modularity purposes: hardware could be designed to perform reassignment of 64 kb/s byte-interleaved channels separately from 16 and 32 kb/s bit-interleaved channels, 2 and 4 kb/s subchannels could be reassigned separately from channels, 16 kb/s channels could be reassigned separately from 32 kb/s channels, and framing and synchronization could be performed in separate hardware from that which performs channel reassignment. Note that an important advantage to function modularity is that the size modularity of each function may be different, allowing a higher degree of configurability.

#### 4.2.2 Size

Size refers to the number of bit streams which the hardware can handle or the number of channels which can be accommodated. It is measured in number of digital groups (T1, AUTOSEVOCOM II and TRI-TAC), channels (64 kb/s byte-interleaved and 16 and 32 kb/s bit-interleaved), and subchannels (2 and 4 kb/s bit-interleaved). Modularity is determined by the size of the increment in channels or digital groups by which the hardware can be reconfigured; the smaller the increment, the greater the modularity. For example, with a modularity of 10 T1 digital groups, the hardware can be configured to any size which is a multiple of 10. Stations with size requirements which are not multiples of this modularity will have some idle hardware. Thus, a station with a size requirement of 15 digital groups would have idle hardware of 5 groups (assuming a modularity of 10) because the hardware would be configured to the increment multiple which is greater than or equal to the requirement (i.e., 20).

#### 4.2.3 DNC Approach

Examination of the DEB multiplex plans and AII trunking requirements reveals that the per station requirements for 64 kb/s byte-interleaved channel reassignment is much larger than that for 16 and 32 kb/s bit-interleaved channel reassignment. Since investigation shows that the former function is less expensive to implement than the latter for a given number of 64 kb/s channels (refer to Section 5.4), a cost savings can be realized by performing the two functions in separate hardware, provided that there is not a large additional overhead and interfacing cost associated with this partitioning. Analysis indicates that this additional interfacing cost will be minimal if the interface between the two hardware units consists of T1 digital groups. Figure 4-2 shows the two hardware units, where the "A" function performs reassignment of byte-interleaved channels and the "B" function performs reassignment of bit-interleaved 16 and 32 kb/s channels and 2 and 4 kb/s subchannels.



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Figure 4-2. Digital Network Control Functional Modularity



Similarly, since the size requirement for 16 and 32 kb/s channel reassignment is larger than that for 2 and 4 kb/s subchannel reassignment and because it is less expensive to implement the former than the latter for a given number of channels, separate hardware is provided for these two functions. Figure 4-2 shows the subchannel reassignment hardware as part of the "B" function because the subchannels are bit-interleaved.

Reassignment of 16 kb/s channels is not performed separately from that of 32 kb/s channels; although the former is more expensive than the latter for a given number of 32 kb/s channels, the size requirements for the latter are smaller. This is the opposite of the previous two functional divisions where the function with the larger size requirement was less expensive. Also, if TRI-TAC goes to a 16 kb/s digitalization rate in the future, then the size requirement for 32 kb/s channel reassignment will go to zero. Hence, since hardware which can reassign 16 kb/s channels can also reassign 32 kb/s channels, these two functions are not performed in separate hardware.

The fourth functional division separates framing hardware from switching hardware. This is desirable because preliminary investigation shows that about half the cost of the DNC hardware will be associated with the framing and synchronization function. Since separation of framing and switching hardware also provides a conceptually simpler design and may allow a simpler implementation of Built-In Test Equipment (BITE). This functional separation is used in the DNC hardware.

The size requirements of the "A" and "B" function are determined from the DEB multiplex plans and from AUTOSEVOCOM II trunking requirements. Table 4-1 presents the maximum size requirements for the two functions. Using the full flexibility deployment algorithm (refer to Section 4.3.4), the multiplex plans reveal that a size modularity increment between 25 and 40 T1 digital groups is desirable, although a more exact figure must await detailed hardware analysis and design (refer to Section 6.2.1).

Modularity for the "B" function is more complex because the trunk groups vary in the number of contained channels. Since the interface of the "A" function (or to DRAMA equipment if the "B" function is deployed without the "A" function) consists of T1 digital groups, this can be used as a measure of size, where a T1 digital group can contain up to 96 16-kb/s channels or 48 32-kb/s channels. Analysis indicates that a size modularity increment from 3 to 5 T1 digital groups is desirable. This is smaller than that for the "A" function because the "B" function is more expensive to implement.

The subchannel reassignment hardware should have a modularity of one T1 digital group, where a T1 digital group can contain up to 768 2-kb/s subchannels or 384 4-kb/s subchannels. However, since this is close to the size requirement, it may be advantageous to make the increment equal to the maximum size requirement.

TABLE 4-1. MAXIMUM SIZE REQUIREMENTS

"A" FUNCTION	64 KB/S CHANNELS			T1 DIGITAL GROUPS
From DRAMA Equipment	3600			150
From "B" Function	-			12
Other (testing, drop, insert, etc.)	96			4
Total	3696			166
"B" FUNCTION	TRUNK GROUPS	CHANNELS	SUBCHANNELS	T1 DIGITAL GROUPS
AII	40	960	960	10
TRI-TAC	10	96	96	2
From "A" Function	-	-	-	12
Other	-	96	96	1
Total	50	1152	1152	25

NOTE: AII and other channels and subchannels are 16 kb/s and 2 kb/s, respectively; TRI-TAC channels and subchannels are 32 kb/s and 4 kb/s, respectively.

### 4.3 NETWORK DEPLOYMENT

Within this section, criteria and rules are discussed for determining the DCS stations at which DNC hardware should be deployed in order to satisfy requirements. The factors affecting the deployment of the DNC-A and/or DNC-B functions (refer to Section 4.2.3 for a discussion of DNC-A and DNC-B functions) at a DCS station are related to both individual station and network-wide requirements. Examples of the former are TRI-TAC and AUTOSEVOCOM II interfacing and circuit breakout for rechannelization. Network-wide requirements relate to the degree of channel reassignment required at each station or selected subsets of stations in order to achieve various levels of control flexibility (e.g., reconfiguration and restoration capabilities).

In the following subsections, four DNC hardware deployment algorithms are discussed which provide different levels of channel reassignment flexibility with regard to network-wide requirements. Figure 4-3 presents the terminology used in the descriptions. Each alternative can establish a circuit between any two stations in the network by utilizing some combination of spare capacity and preempted channels. They differ with regard to the restrictions they place on this capability. Individual station requirements are accounted for in the deployment algorithms by forcing certain stations to contain the desired DNC function.

Section 4.3.5 discusses the general considerations involved in selecting a particular deployment alternative for a specific network and Section 8 illustrates the application of each alternative to a selected subset of the European DCS.

#### 4.3.1 Partial Interconnect

Partial interconnect is the most restricted of the four capabilities with respect to channel connection flexibility. It allows a circuit to be established between any two stations, but the route is predetermined and cannot be selected. Also, the first-level multiplexer ports which terminate the circuit cannot be chosen. This means that manual patching may be required at the two stations which terminate the circuit in order to connect the users to the proper ports. Partial interconnect can establish at least 24 such circuits between any two stations.

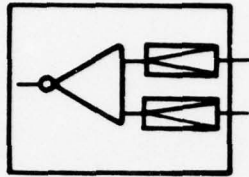
To provide partial interconnect, DNC hardware must be placed at stations such that the following conditions are satisfied:

- a. For each station at least one digroup which terminates at that station must pass through at least one station equipped with DNC hardware.



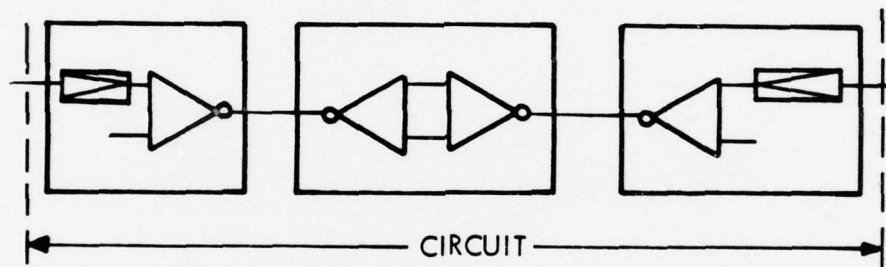
- STATION - A TCF OR PTF

EXAMPLE :



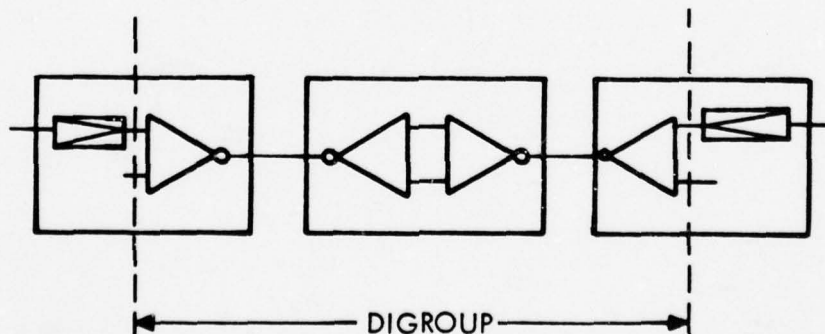
- CIRCUIT - A 64 kb/s CONNECTION BETWEEN TWO TD-1192 CHANNEL PORTS

EXAMPLE :



- DIGROUP - A 1.544 Mb/s CONNECTION BETWEEN THE LINE SIDES OF TWO TD-1192 MULTIPLEXERS

EXAMPLE :



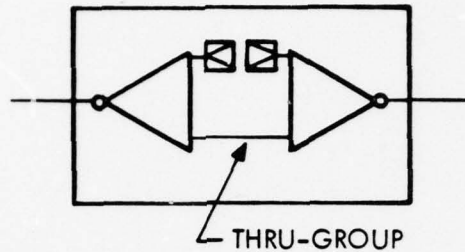
- ROUTE - A SERIES OF STATIONS DESCRIBING THE PATH THROUGH THE NETWORK OF A CIRCUIT OR DIGROUP

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Figure 4-3. Network Terminology (Sheet 1 of 2)

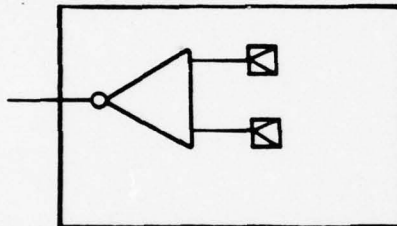
- THRU-GROUP - A DIGROUP WHICH PASSES THROUGH A STATION AT THE T1 LEVEL WITHOUT BREAKOUT

EXAMPLE :

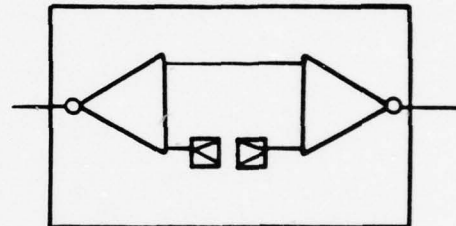


- TERMINAL STATION - A STATION WITH CHANNEL BREAKOUTS

EXAMPLES :

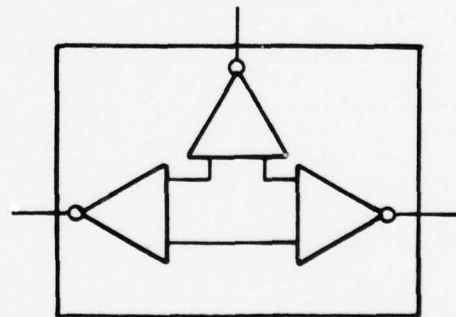
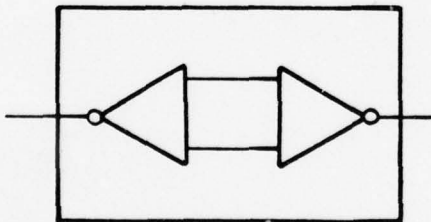


OR



- REPEATER STATION - A STATION WITH NO CHANNEL BREAKOUTS

EXAMPLES :



- BRANCHING STATION - A STATION WITH THREE OR LINKS

LEGEND :

TCF OR PTF



TD-1193



TD-1192



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Figure 4-3. Network Terminology (Sheet 2 of 2)

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DIGITAL NETWORK CONTROL.(U)  
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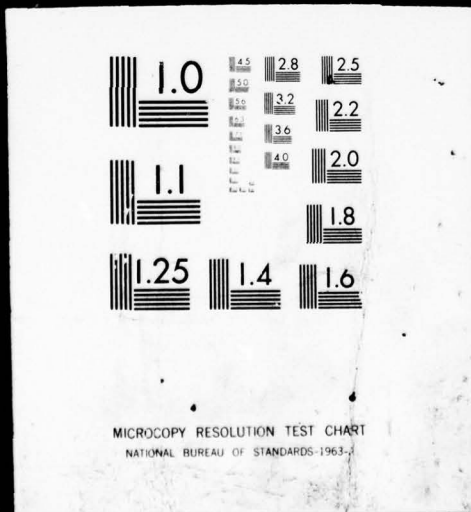
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- b. All stations with DNC hardware and the digroups which pass through the hardware must form a connected graph where the stations are nodes and the digroups are edges.

Partial interconnect provides a network reconfiguration capability in that circuits can be established between two stations by using existing routes or creating new ones. Note that the capacity for the circuit must exist before DNC can connect this capacity together as a new route. This could be spare capacity or could involve preemption of a lower priority circuit. Partial interconnect provides a very limited rerouting capability because only a few routes through the network are used. Also, its use in network performance assessment and fault isolation is limited because of the relatively few digroups which pass through DNC hardware.

#### 4.3.2 Full Interconnect

Full interconnect is a more flexible scheme than partial interconnect because the first-level multiplexer ports at the terminating stations for the circuit can be specified. In other words, a circuit can be established between any two first-level multiplexer ports while partial interconnect can only establish a circuit between some first-level multiplexer ports. However, the route is predetermined and cannot be specified, as with partial interconnect.

In order to provide full interconnect, all digroups in the network must pass through at least one station with DNC hardware. Additionally, the connected graph condition mentioned for partial interconnect must be met. This results in a greater number of stations being equipped with DNC hardware than with partial interconnect.

Full interconnect provides an increase in the ability to provide DNC functions. No manual patching is required at stations to perform DNC functions, as is the case with partial interconnect. Since more digroups pass through channel reassignment hardware, there is greater flexibility in network reconfiguration and in rerouting. Note that not all routes are used by full interconnect, so the rerouting capability is still limited. Performance assessment is enhanced since all digroups pass through DNC hardware, but fault isolation using loopback is still restricted because many digroups only pass through one station with DNC hardware.

#### 4.3.3 Partial Flexibility

Similar to partial interconnect in that the terminating first-level multiplexer ports cannot be chosen, partial flexibility adds the capability to select any route through the network. As mentioned previously, manual patching may be required at the terminal stations of the circuit.

Partial flexibility can be provided by deploying DNC hardware to satisfy these conditions:

- a. For each station at least one digroup which terminates at that station must pass through at least one station with DNC hardware.
- b. All branching stations must have DNC hardware.
- c. All chains of one or more two-link terminal stations must have DNC hardware deployed such that a thru-group through the chain can be created.
- d. The connected graph condition discussed in Section 4.3.1 must be met.
- e. If a terminal station has a link which consists only of thru-groups, then DNC hardware must be deployed at that station in order to connect one digroup in that link to a TD-1192.

Condition c. is required in order to account for the situation illustrated by example A in Figure 4-4. There is no way to establish a circuit between stations A and C via B unless DNC hardware is deployed at station B. This follows as a result of B having no thru-groups. A more complex case is shown in example B of Figure 4-4. Here, both two-link terminal stations have thru-groups but DNC hardware is still required at B or C in order to establish a circuit between A and D. The conditions just described are sufficient to provide partial flexibility, but are not necessary. If an additional constraint is placed on the definition of partial flexibility, that no circuit pass through the same station more than once, then these conditions become necessary and sufficient.

Partial flexibility provides a more powerful rerouting capability than the two previous alternatives because any route through the network can be specified. However, manual patching may be necessary at the terminating stations for the circuit. This is illustrated in example C of Figure 4-4. As shown in this figure, if a circuit from A directly to B is to be rerouted via C, then manual patching must be performed to connect the users at A and B to this alternate circuit. This manual patching requirement also limits the network reconfiguration capability. The fact that only a few digroups pass through DNC hardware also limits the network reconfiguration capability as well as the performance assessment capability. For those digroups which do pass through DNC hardware, the fault isolation capability is enhanced over partial and full interconnect because a higher percentage of the digroups pass through DNC hardware more than once.



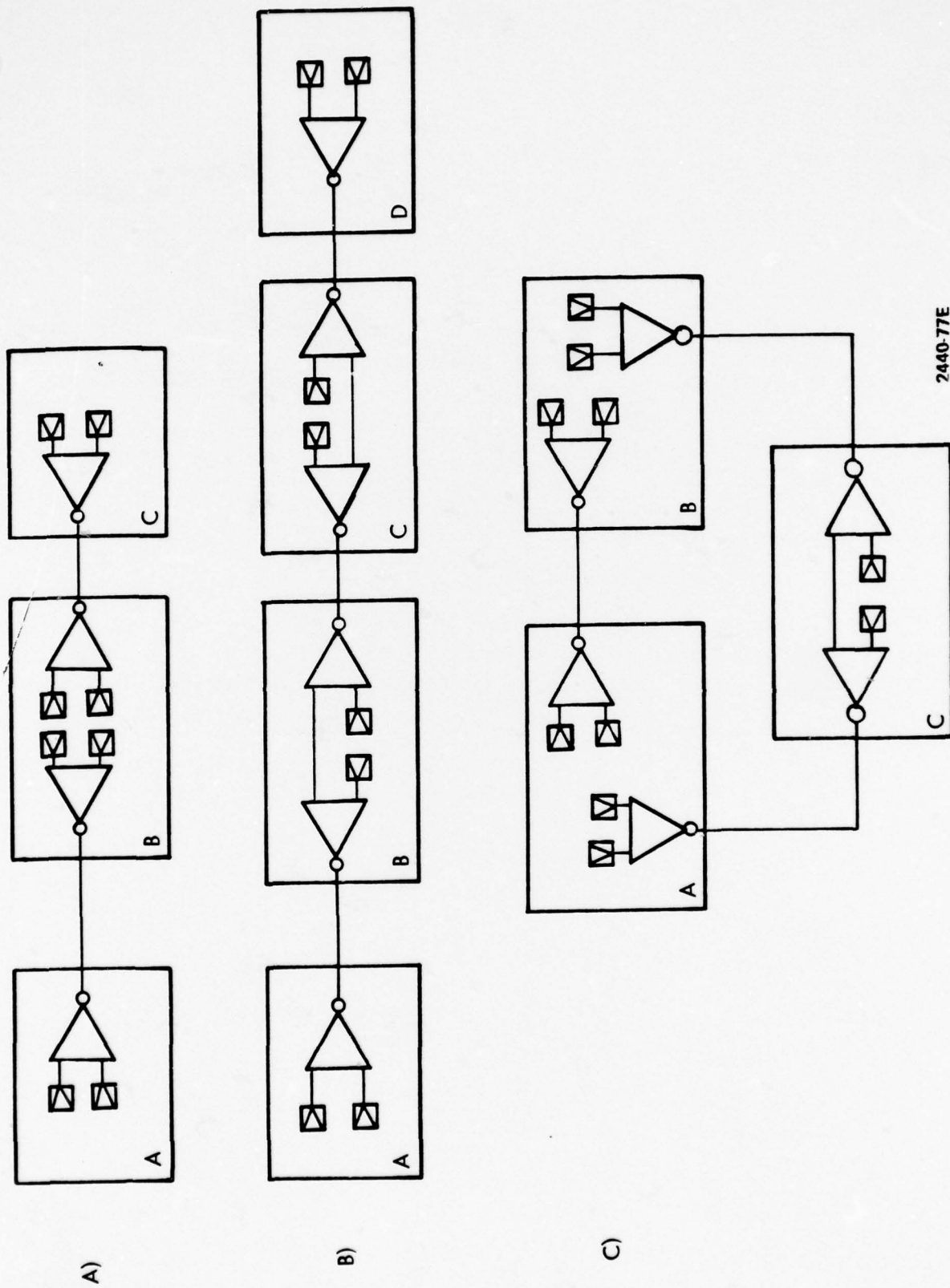


Figure 4-4. Partial Flexibility Examples

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#### 4.3.4 Full Flexibility

This is the most flexible of the four capabilities. It provides the benefits of full interconnect and partial flexibility in that the first-level multiplexer ports which terminate the circuit can be selected as well as the route through the network.

To provide this capability, DNC hardware is required at all stations except non-branching repeaters and one-link terminal stations. Again, the connected graph condition discussed in Section 4.3.1 must be met. As with partial flexibility, the addition of the constraint that no circuit pass through the same station more than once makes these conditions necessary and sufficient.

Full flexibility provides a complete spectrum of reconfiguration, rerouting, testing, and loopback capabilities. All possible routes in the network can be utilized with no manual patching required at the terminal stations. In example C of Figure 4-4, DNC hardware located at A and B would automatically connect the users to the alternate circuit established via C, as discussed in Section 4.3.3. All circuits and digroups can be tested and looped back, since all pass through DNC hardware and many circuits pass through such hardware at more than one site. An improvement in network performance assessment and fault isolation over full flexibility can be obtained by also placing DNC hardware at one-link terminal sites. A slight improvement can also be obtained by equipping non-branching repeater stations, but this would require the deployment of TD-1193s at these stations and hence is not cost-effective.

#### 4.3.5 Network Application

In Sections 4.3.1 through 4.3.4, four channel reassignment alternatives and related DNC hardware deployment algorithms are discussed. The alternatives in increasing order of capability are as follows:

- a. Partial Interconnect
- b. { Full Interconnect
- { Partial Flexibility
- c. Full Flexibility

Full interconnect and partial flexibility are ranked equally even though their capabilities differ. While partial flexibility provides a superior rerouting capability over that for full interconnect, its network reconfiguration and performance assessment capabilities are more limited. Thus, the alternative chosen for a particular situation would depend on the requirements.

In general, the benefits that the DCS derives from DNC with respect to transmission capacity utilization, network reconfiguration, network flexibility, interoperability with TRI-TAC, and system control operations increases with increasing reassignment capability; however,

as channel reassignment capability increases so does the cost of providing DNC since its hardware deployment requirements increase accordingly, as discussed fully in the four previous subsections.

To properly assess the value of the various channel reassignment capabilities to the DCS and system control, it is clear that the benefits and related costs of DNC within its operational environment must be quantified. In addition, since DNC has the potential for transmission equipment and manpower savings and increased transmission capacity utilization, it is necessary to define the exact relationship and sensitivity of these savings to the channel reassignment alternatives as a prelude to selecting a particular alternative. Once this cost relationship is fully determined, it is then possible to select the desired level of DNC application by trading off cost for operational performance, survivability and availability.

Clearly, such a cost/benefits analysis with respect to the European DCS is beyond the scope of this study. However, Section 8 illustrates the application of DNC to a selected subset of the European DCS.

#### 4.4 SYNCHRONIZATION

This section establishes the synchronization requirements to be imposed on DNC hardware in order to ensure that channel reassignment causes no significant performance degradations in digital groups with respect to frame synchronization and Bit Count Integrity (BCI). A discussion of the methods and algorithms employed to satisfy the requirements is provided in Section 6.2.4.

Two aspects of synchronization are pertinent to the problem at hand. One is master frame synchronization and the other is nodal timing. The issues and requirements within each area are discussed below.

##### 4.4.1 Master Frame Synchronization

As discussed in Section 4.1.4, DNC hardware will be deployed between the first- and second-level multiplexers. At this hierarchical level, all bit streams with which DNC hardware will interface appear as either T1 digital groups (D2/D3 compatible [Reference 4-1], or TRI-TAC formatted digital groups [Reference 4-2]).

All digital groups formed by time division multiplexing lower rate groups or channels are comprised of contiguous master frames. Figure 4-5 illustrates the master frame structure for both T1 and TRI-TAC formatted digital groups. The former contains 24 byte-interleaved channels (plus one synchronization bit) and has a period of 0.125 msec. The latter contains between 8 and 144 bit-interleaved channels and has a fixed period of 0.5/0.25 msec. (for 16 kb/s/32 kb/s digitalization rates, respectively).



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Figure 4-5. Digital Group Frame Structure

The first bit of each master frame is used for synchronization. In the T1 digital group, the bit is shared between framing and signaling. Thus, the resultant framing period is 0.25 msec, which equates to a frame rate of 4 kHz. In TRI-TAC formatted groups, the first bit of each master frame is devoted solely to framing; signaling is performed with common channel interswitch signaling messages. Thus the framing period equals the master frame period in this case. The framing pattern in the T1 and TRI-TAC formatted groups is identical, namely, an alternating pattern of ones and zeroes (101010....). Note that T1 groups and TRI-TAC groups based on the 32 kb/s digitalization rate have identical framing patterns and rates. As discussed in Section 3.2.4, this precludes inputting such a TRI-TAC group directly into a TD-1192 since it could interfere with the multiplexer's synchronization.

In each master frame, the location of each channel is only known relative to the starting position (framing bit) of the master frame. Therefore, in order to accomplish channel reassignment, DNC hardware must be able to establish and maintain master frame synchronization in each digital group to which it is connected. Implicitly assumed is the fact that the digital groups are unencrypted. Bulk encryption precludes channel reassignment, as discussed in Sections 4.1.3 and 4.7. Based on the foregoing, the requirements imposed on DNC hardware with respect to framing are shown in Tables 4-2 and 4-3. These tables are identical to the synchronization requirements established for the hardware with which the DNC interfaces, the TD-1192, the TD-1193, and various TRI-TAC equipment. Note that the TD-1192 utilizes a unilateral framing procedure while TRI-TAC utilizes a bilateral procedure.

A major consideration is that the inclusion of DNC hardware which meets the specified framing requirements does not increase the mean time to acquire synchronization in a circuit following loss of BCI due to a bit stuffing error in a TD-1193. Since the DNC hardware will synchronize to each terminating digital group, there is no attendant increase in the mean time to acquire synchronization.

#### 4.4.2 Nodal Timing

All digital groups which pass through DNC hardware will undergo channel reassignment via a synchronous switching technique (refer to Section 5). Thus, it is necessary to keep the bits within these groups in frequency synchronization with the DNC timing supply in order to maintain BCI.

There are two general requirements which if met will ensure maintenance of BCI.

- a. All digital groups passing through DNC hardware must be in relative frequency synchronism.
- b. DNC must maintain frequency synchronization with the digital groups.

TABLE 4-2. DNC/TD-1192 AND TD-1193 FRAME SYNCHRONIZATION REQUIREMENTS<sup>1</sup>

	REQUIREMENT
A. FRAME ACQUISITION	
I. Start-Up	
1. Time to Acquire Sync	<u>&lt;</u> 50 msec
2. Probability of Acquiring Sync	.90
3. Probability of False Acquisition	Not Specified
II. Following Loss of BCI (less than <u>±</u> 2 bits)	
1. Time to Detect and Reacquire	<u>&lt;</u> 50 msec
2. Probability of Acquiring Sync	.90
B. FRAME MAINTENANCE (BCI MAINTAINED)	
1. Mean Time to False Loss-of-Sync	<u>&gt;</u> 6 Hours

NOTE: 1. Based on Reference 4-3.



TABLE 4-3. DNC/AUTOSEVOCOM II AND TRI-TAC FRAME  
SYNCHRONIZATION REQUIREMENTS<sup>1</sup>

A. FRAME ACQUISITION (MSEC)	AN/TTC-39		OTHER TRI-TAC ELEMENTS	
	AUTOSEVOCOM II <sup>2</sup>	TRI-TAC	@16 KB/S	@32 KB/S
1. Loss of Frame Detection	600 <sup>3</sup>	600 <sup>3</sup>	100	100
2. Frame Request Detection	150	100	150	100
3. Frame Acquisition	150	100		
4. Mission Stream Format Detection	150	100		
B. FRAME MAINTENANCE				
1. Mean Time to False Loss-of-Sync <u>&gt;</u> 240 Hours				

- NOTES: 1. Based on Reference 3-2
2. Assuming AUTOSEVOCOM II uses the same frame synchroni-  
zation control procedures and algorithms as TRI-TAC
3. Includes 500 msec flywheel.

The first requirement will be realized following the introduction of AUTOSEVOCOM II service in the European DCS. It is necessary that the DCS go synchronous at this time (or employ highly stable asynchronous clocks) since AUTOSEVOCOM II is a synchronous circuit switching network. The first requirement may also be realized prior to full AUTOSEVOCOM II service depending upon the way in which the present AUTOVON system transitions to AUTOSEVOCOM II. That is, there may be regions or areas of synchronous service realized with DAXs and AN/TTC-39s which satisfy the first requirement. In any event, DNC will be employed only at those DCS stations where a. is satisfied.

The second requirement will be satisfied by slaving each DNC timing supply to an AUTOSEVOCOM II nodal timing supply or an approved digital group. Thus all timing signals needed to perform DNC functions at a station will be synthesized from a timing signal standard derived from the AUTOSEVOCOM II timing subsystem or equivalent highly stable DCS source.

In Section 6.2.4, the DNC timing supply stability is determined. It is based on a free-running requirement of 24 hours as specified by DCEC during Task VI of the study.

#### 4.5 MAN/MACHINE INTERFACE

This section discusses the interface between human personnel and the hardware and software which are the implementation of Digital Network Control. The goal of any such interface is to permit man and machine to exchange information in a meaningful way so as to aid in the accomplishment of a higher-order mission, which in this case is system control of the digital DCS. An important consideration is the difference in abilities between man and machine. Man excels at interpreting complex patterns while the equivalent computer capability is still in its infancy. Machines, however, are much faster than man at most other communications tasks, such as reading and writing. A well-designed interface makes use of the different capabilities of man and machine in order to increase the efficiency of the interface in performing its function.

The man/machine interface can be divided into two parts: the physical interface and the information interface. The physical interface refers to the hardware required to transduce information between forms which are perceptable by the machine, such as electrical signals, and forms which are perceptable by man, such as audio and visual signals. The information interface refers to the syntactic and semantic (i.e., structure and meaning) of the information which flows across the interface. Two types of information interfaces can be identified: interactive communications and non-interactive communications. Interactive communications are two-way dialogues between man and machine whereas non-interactive communications are one-way. Section 4.5.1 describes the physical interface, Section 4.5.2 discusses interactive communications, and Section 4.5.3 discusses non-interactive communications.

#### 4.5.1 Physical Interface

The hardware which makes up the physical interface provides the actual link between man and machine. It consists of hardware to pass information from man to machine and vice versa. An important principle of human engineering is that these equipments be colocated. This permits the man to receive data rapidly concerning any actions he has taken. For example, if the man is manipulating a knob which controls some output level as measured by a meter and, if the meter and knob are not colocated, there will be a considerable delay between the man's action of rotating the knob and his learning of the effect of this action on the output level. He learns of this effect either by receiving a message from someone stationed near the meter, or by moving himself to the meter's location and observing it. In either case, any incorrect setting made will be in force throughout this delay. Colocating the knob and meter allows a much shorter delay in the feedback loop, which in this case is man. Incorrect settings are corrected more rapidly, resulting in better system performance.

Similar reasoning indicates that if ATEC is deployed, then DNC should make use of ATEC man/machine interface hardware, such as the Controller Terminal Function (CTF) and the Alarm Reporting Function (ARF). ATEC is analogous to the meter in the previous example in that it measures the performance levels of the DCS. In this example, DNC is similar to the knob, because it provides a means of controlling the DCS in order to change its performance levels (e.g., rerouting a circuit from a failed link to an operational link). A cost savings is also realized because duplicate equipment is eliminated. However, if ATEC is not deployed, then a man/machine interface must be developed for DNC.

The physical man/machine interface for stand-alone DNC is similar to that for ATEC. The main communications device is the Keyboard Display Unit (KDU). This consists of a CRT display capable of presenting alphanumeric characters and a keyboard for entry of information. The keyboard transduces human-perceptable data into machine-perceptable data while the display performs the reverse function. The display also echoes characters entered via the keyboard back to the man for rapid identification of errors. A printer accompanies the KDU to provide a hard copy of the information on the display. An alarm status panel is also provided and uses lights and a tone generator to indicate trouble with the DNC hardware.

#### 4.5.2 Interactive Communications

Interactive communications are two-way dialogues between man and machine. It is basically a feedback system where man and machine interact with one another to accomplish a task. Section 4.5.2.1 discusses the syntax of the dialogue as it applies to the KDU. Section 4.5.2.2 describes the semantics of the dialogue as it applies to the DNC and outlines the types of commands which DNC software must support.



#### 4.5.2.1 Interactive Syntax

The man/machine interface is a stimulus/response system in that the man initiates a dialogue by typing something on the keyboard (stimulus) and the machine analyzes the information and produces output on the display (response). The lowest level of interaction is that between the man and the KDU functions of character entry, cursor control, and editing. The man enters characters by typing on the keyboard (stimulus) and the characters are echoed on the display (response). By using editing functions such as character delete and line delete, the man can remove characters from the display. The cursor, a blinking square on the display, indicates to the man where characters which are typed will appear. For example, to type a line of characters the man would position the cursor at the beginning of a blank line (e.g., by using the RETURN key) and begin entering characters. The cursor moves one position to the right with each character typed. To insert characters into an existing line the cursor is positioned at the desired location (e.g., using the ↑, ↓, ←, → keys) and the characters to be inserted are typed. Characters to the right of the cursor are moved to the right one position for each inserted character. Characters which are moved "off" the right-hand edge of the display will appear on the next line, starting at the left-most position. Note that if the ATEC CTF is used as the man/machine interface, then these character entry and modification functions may be different, but the end result will be the same. These functions all take effect on characters in a command to the DNC software prior to the interpretation of the command by the software. When the man is satisfied that the typed command is accurate, he transmits it to the software by pressing the RETURN key.

The general format of a command is as follows:

COMMAND-NAME	PARAMETERS	OPERANDS
--------------	------------	----------

where command-name indicates which command is to be executed, parameters indicate variations in the execution, and operands are inputs to the command execution. When a command is entered, the machine checks to see if the command is legal. If not, it generates an error message to the man; otherwise it executes the command and returns an appropriate response. Responses take the following format:

MESSAGE-NUMBER	MESSAGE-DESCRIPTION
----------------	---------------------

where message-description provides a brief explanation of the machine's response, such as "ILLEGAL COMMAND NAME" and the message-number acts as an index to more detailed descriptions either maintained on-line or in a document.

#### 4.5.2.2 Interactive Semantics

A higher degree of interaction occurs at the semantic level. Three types of communications at this level can be identified based on the function to be accomplished: information entry, information modification and information retrieval. Information entry refers to a

primary flow of data from man to machine, such as creating or adding to a data base. Information modification includes functions such as editing and commands which cause changes in stored information with the goal to alter external parameters such as channel connectivity. Information retrieval is characterized by a primary flow of information from the machine to man. This level provides for reversed stimulus/response dialogues in that the machine may present a stimulus. For example, if the man enters a command the machine's response may be a prompt (stimulus) for the man to enter more information (response).

Information entry commands involve creation of, and addition to, the data base required for DNC. This data base contains information such as channel connectivity through DNC hardware, and how the digital groups are connected to this hardware. If ATEC is deployed, DNC will utilize the commands for entry of data into the ATEC data base, modified appropriately so as to handle the DNC data base. If ATEC is not deployed then these functions must be implemented for DNC. These commands will cause the machine to prompt the user for various data as the data base is built up.

Information modification is the most frequently used dialogue for DNC. Most of the commands in this category are aimed at altering external parameters, although commands similar to those for information entry are provided for updating the data base. Commands to perform DNC functions such as rerouting, should have command names which are meaningful to the human personnel who use them. Table 4-4 presents the command names which are chosen to perform the functions of DNC. DNC software must be flexible enough to handle additions to or changes in this list.

TABLE 4-4. COMMANDS

NAME	DNC FUNCTIONS
REROUTE	Reroute a channel, subchannel, or digital group to restore service.
MONITOR	Bridge a channel, subchannel, or digital group to monitor it.
TEST	Connect a channel, subchannel, or digital group to test equipment.
LOOPBACK	Loopback a channel, subchannel, or digital group.
ASSIGN	Assign a channel, subchannel, or digital group to another for purposes of network reconfiguration, AII and TRI-TAC interfacing, elimination of backhauling, etc.

Information retrieval commands provide personnel with the ability to obtain information from the DNC data base. Again, if ATEC is deployed then DNC will use its retrieval commands; otherwise, similar commands must be devised for DNC. These commands allow personnel to obtain channel connectivity information and DNC hardware status. The commands use prompting from the machine whenever complex data base records are being accessed.

#### 4.5.3 Non-interactive Communications

Non-interactive communications are one-way dialogues, the most important example of which is alarms. When a failure in the DNC hardware or software is detected an alarm is generated. This results in a message being displayed on the KDU to indicate what occurred and to describe any automatic correction action taken by the hardware. A light is lit on the alarm status panel and blinks until the alarm state is acknowledge, at which point the light becomes steady on. Simultaneously, a tone generator creates an audible signal which persists until the condition is acknowledged. When the fault condition is rectified, the light is turned off.

Two other non-interactive communications provide machine input/output. A printer provides hard copy output for the machine. If a teletype were used, it could also accommodate interactive dialogues. A high-speed input device such as a magnetic or paper tape reader is required to load large quantities of information into the DNC processors. An example would be the loading of data base during system startup or recovery.

#### 4.6 AVAILABILITY

This section establishes an availability requirement for DNC hardware based upon the channel and digroup availability requirements established in TR12-76 (Reference 4-3).

The DCA has placed an availability requirement upon the reference digroup shown in Figure 4-6. This reference digroup is defined as two second-level multiplexers with associated bulk encryption equipment connected by three tandem RF links. If the three links are LOS, the reference digroup is denoted a Type A; if two of the links are LOS and one is troposcatter, it is denoted a Type B. The DCA established availability requirements are 0.9998 for the Type A reference digroup and 0.9997 for the Type B reference digroup.

The DCA reference channels are shown in Figure 4-7. The 64 kb/s PCM channel is defined as two first level multiplexers interconnected by four Type A reference digroups and one Type B reference digroup. The 16/32 kb/s channel extends the PCM reference channel through two submultiplexers. The required availability of both reference channels is 0.999.



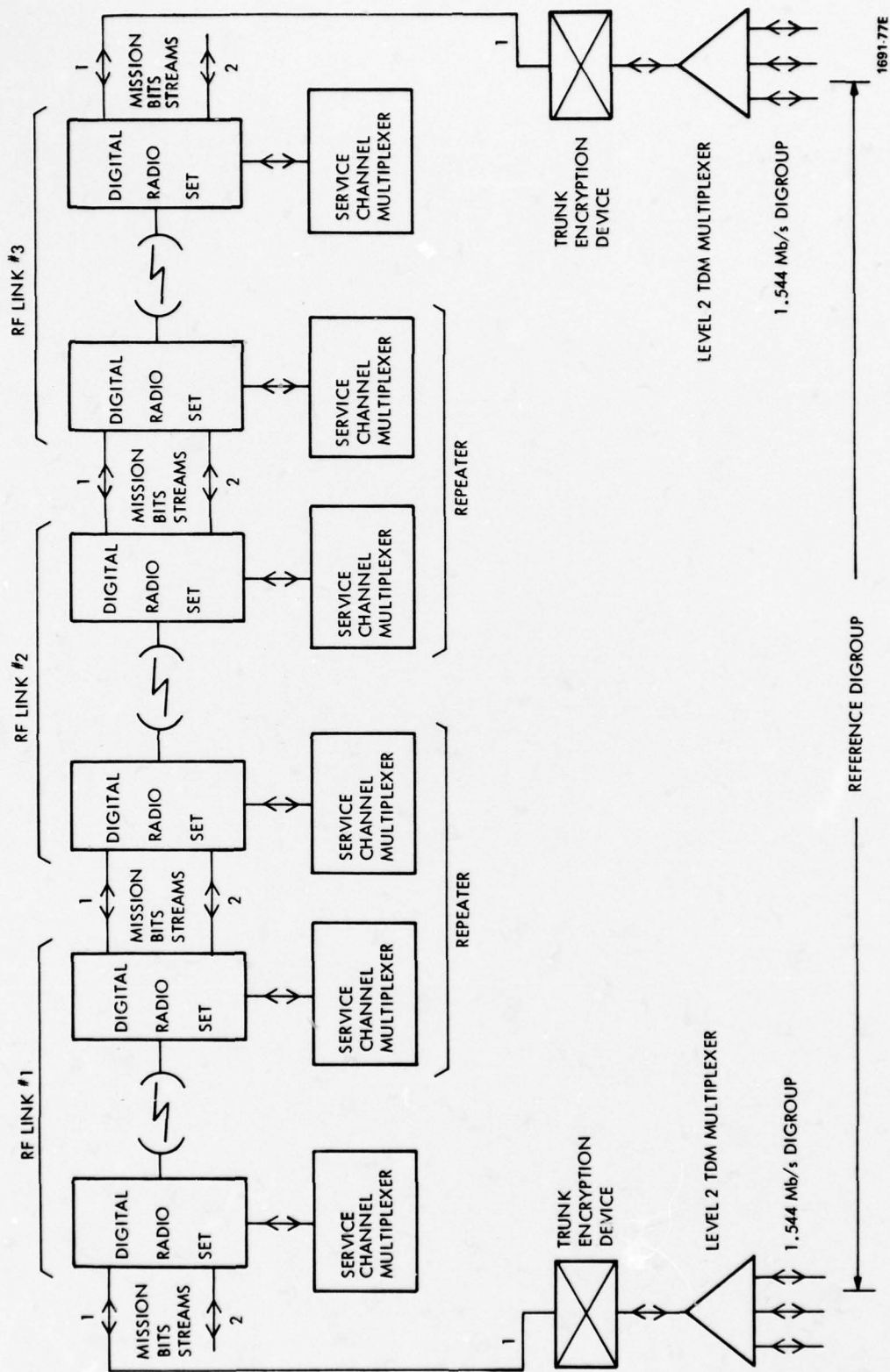


Figure 4-6. Reference Digroup

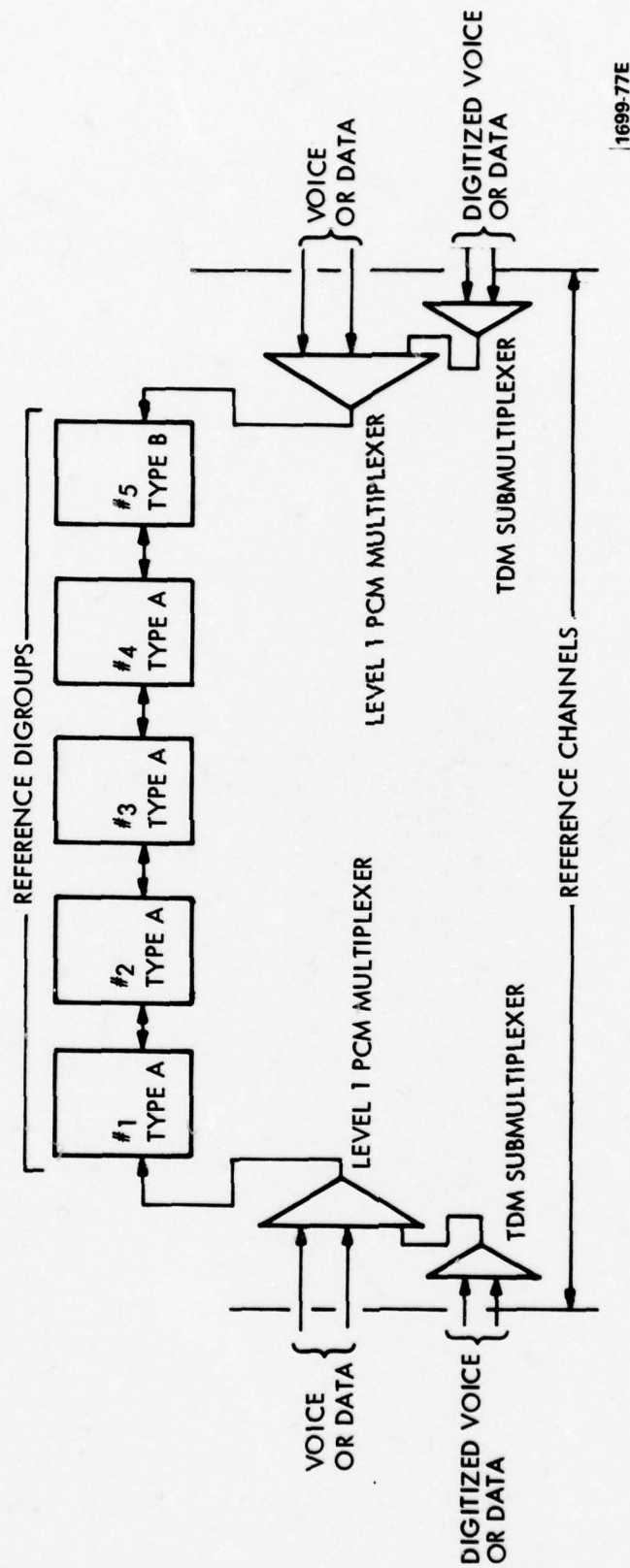


Figure 4-7. Reference Channels

In general, the application of DNC to the DCS will improve channel availability due to the diversity routing that channel reassignment provides. However, the DNC availability requirement will be established for the worst case situation in which alternating routing is not possible. Thus, DNC hardware appears as a series element in the reference channels and has a series impact on their availability. In order that DNC does not significantly degrade channel performance, it is proposed that DNC hardware not increase reference channel unavailability by more than a factor of five percent. Thus, the maximum unavailability contribution to the reference channels due to DNC is required to be less than or equal to  $0.05 (1 - 0.999) = 0.00005$ .

The above unavailability requirement is due to the contribution of all DNC hardware in the reference channel. The unavailability allocation on a per station basis is a function of the number of stations at which DNC is deployed. As may be seen in Figure 4-7, both reference channels pass through 16 stations. However, only six stations provide access at the digroup level. Using this value, the DNC unavailability requirement on a per station basis and referenced to the channel level is  $0.00005/6 = 8.33 \times 10^{-6}$ . This translates into an availability requirement of  $1 - 8.33 \times 10^{-6} = 0.99999167$ .

#### 4.7 COMSEC CONSIDERATIONS

This section discusses the interaction between DNC hardware and COMSEC hardware for both the DCS and TRI-TAC. The use of encryption for security purposes places several constraints on the use of DNC, depending upon at which level in the multiplex hierarchy the encryption device is located. DNC has a small impact on the operation of encryption hardware which is also dependent upon its location in the multiplex hierarchy.

##### 4.7.1 Channel Level Encryption

Channel level or end-to-end encryption occurs when the encryption device is located at or near the users' terminal. Two examples are the Digital Subscriber Voice Terminal (DSVT) and the KY-3. Channel level encryption of 64, 32, and 16 kb/s channels does not pose any problems for DNC because DNC hardware does not depend upon the information contained within the channel. Each channel is merely a bit stream to be reassigned. The exception is the overhead channel used in AUTOSEVOCOM II and TRI-TAC communications because it contains subchannels which are subject to reassignment. This does not present a problem since overhead channels are not encrypted at the channel level.

DNC does have an effect on the operation of end-to-end encryption. If an encrypted channel is rerouted, it is likely that bit count integrity will be lost due to a change in the length of the path which the circuit traverses. Hence, the channel encryption devices will have a resync. This is not a serious consideration because most events which lead to rerouting, such as an equipment failure, also cause a loss of BCI or possibly total loss of communications.



#### 4.7.2 Group Level Encryption

Group level encryption refers to bulk encryption of T1 digital groups, such as with the CY-104 used in FKV and DEB I, and of AUTOSEVOCOM II and TRI-TAC trunk groups. DNC hardware cannot reassign channels within encrypted groups because the framing pattern cannot be located within the groups due to the encryption. Hence, encrypted groups can only be group-reassigned, that is, an encrypted group can only be patched at the group level by the DNC hardware. Note that if an encrypted group is rerouted, BCI will be lost and the cryptos will have to resynch, as discussed for channel level encryption.

#### 4.7.3 Supergroup Level Encryption

Supergroup level encryption is bulk encryption between a second-level multiplexer and a radio. The crypto device used in DEB Stages II, III and IV is the KG-81 which accepts supergroup rates of 3.168, 6.336, 9.504, and 12.672 Mb/s. Since the KG-81 is deployed at a higher level in the multiplex hierarchy than is DNC hardware, it presents no problems because the DNC hardware is located on the clear side of the crypto. Also, channel reassignment does not affect crypto sync because it does not cause loss of supergroup BCI.

#### 4.8 DNC SCHEDULING

Up to this point in Section 4, the preferred application of DNC to the European DCS has been determined. This section examines the factors affecting the scheduling of DNC. Figure 4-8, Related Program Milestones, provides a baseline for discussing the introduction of DNC into the DCS.

Based on the results of previous sections, there are two factors which constrain the application and in turn the scheduling of DNC. The first is that channel reassignment can only be employed in unencrypted digital groups (refer to Section 4.7). This precludes the introduction of DNC until interim operational capability (IOC) for DEB Stage II, since DEB Stage I encrypts at the T1 level. This is not a serious limitation since DEB Stage I affects only a small portion of DCS Europe. The second factor is that the digital groups in which reassignment is to be performed must be in frequency synchronism (refer to Section 4.4.2). Since synchronous transmission is a basic requirement for the AUTOSEVOCOM II network, DNC applicability is assured for no later than IOC for the European AUTOSEVOCOM II network. However, this does not preclude the introduction of DNC prior to this time. Present plans call for the DCA to examine the feasibility of providing thin line or regions of AUTOSEVOCOM service prior to the availability of the AN/TTC-39. Such an arrangement would provide timing of sufficient stability to permit DNC deployment in a limited fashion as early as 1980 (the expected availability of DAXs). Additionally, the DCS timing system presently in planning could be operational well before AUTOSEVOCOM II IOC. This would permit unlimited DNC application to occur jointly.

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Figure 4-8. Related Program Milestones

It is clear that DNC introduction into the DCS must await the availability of a suitable timing network, but can occur no earlier than 1978 which is when DEB Stage II sees initial operation.



## SECTION 5

### CHANNEL REASSIGNMENT TECHNIQUE SELECTION

Four switching techniques are evaluated to determine the optimal method for providing a channel reassignment capability as described in Section 4. A set of design constraints is used to select the candidate techniques which are then analyzed and compared according to a set of evaluation criteria. Section 5.1 discusses the selection and evaluation processes and associated criteria. Section 5.2 describes each of the four techniques and the baseline configurations used in the evaluation. Section 5.3 presents the results of the analysis and indicates the selected approach, and Section 5.4 extrapolates these results to the 16/32 kb/s case.

#### 5.1 EVALUATION CRITERIA

The analysis is a two-step process consisting of a definition phase and an evaluation phase. During the definition phase a set of design constraints is used to select the four candidate techniques and to develop initial configurations for each technique to be used in the evaluation phase. These configurations are then evaluated and the results weighted and compared. Factors common to all approaches, such as frame synchronization and alignment, are not considered in this evaluation nor are factors not directly involved in the channel reassignment function implementation, such as the man/machine interface. The analysis is performed for 64 kb/s PCM channels and extrapolated to the 16/32 kb/s case.

##### 5.1.1 Design Constraints

Table 5-1 summarizes the design constraints used in the first phase of the analysis. These constraints must be met in order to provide a channel reassignment capability. The technique must be fast enough to handle 1.544 Mb/s digital groups in the T1 format containing 24 64-kb/s PCM channels. During a reassignment operation Bit Count Integrity (BCI) must be maintained on all channels not involved in the reassignment, but BCI may be lost on the channels being reassigned. The technique must be strictly non-blocking (i.e., any connection can be made at any time) as opposed to most circuit switches where blocking is permissible. This is to allow flexibility in rerouting and to prevent a situation where a reroute cannot be terminated because the pattern of active reroutes blocks the normal connection.

##### 5.1.2 Evaluation Factors

The goal of this channel reassignment technique selection is to minimize the total system cost; to this end, five factors are identified which are affected by the choice of channel reassignment technique and which in turn impact the system cost. Table 5-2 presents the evaluation factors used in the second phase. Each

impacts the total cost of a channel reassignment device and is given a weight according to its impact. Each technique is given a score from one to ten in each category. The scores are then multiplied by the weight for that category and summed to give an overall weighted score for each technique.

Equipment cost is a major factor and contributes directly to system cost. R/M/A affects manpower utilization and the supply of spare parts which must be stocked. Additionally, the availability of the device must be such that DCS availability is not degraded below specifications. Control complexity reflects the cost of the control software and of the processor to run it. Modularity determines the ease with which an operating device can be expanded and also determines the amount of idle equipment for a given size configuration. Size and power impact the power supply, mounting hardware, cabling requirements, and floor space requirements.

TABLE 5-1. DESIGN CONSTRAINTS

FACTOR	CRITERIA
Speed	Must handle 64 kb/s PCM channels
Bit Count Integrity	Must maintain BCI on channels not being reassigned
Non-blocking	Must be strictly non-blocking

TABLE 5-2. EVALUATION FACTORS

FACTOR	WEIGHT	CRITERIA
Equipment Cost	1.0	Minimize
R/M/A	0.9	Maximize MTBF, availability Minimize repair time
Control Complexity	0.7	Minimize
Modularity	0.5	Maximize ability to configure and reconfigure
Size and Power	0.3	Minimize

## 5.2 TECHNIQUE DESCRIPTIONS

The four techniques chosen are representative of those current switching techniques capable of performing channel reassignment and of meeting the design criteria discussed in Section 5.1.1. The techniques are: Digital Space Division Switching (DSDS), Digital Time Division Switching (DTDS), Software Directed Switching (SDS), and Combined Space-Time Switching (CSTS). The basic principles of operation of each technique are described and a baseline configuration is selected.

### 5.2.1 Digital Space Division Switching (DSDS)

DSDS is the extension of analog space division switching to digital systems. Logic gates control the flow of digital signals at the channel level just as crosspoints control the flow of analog signals in many current circuit switches, such as the GTE Sylvania Electronic Tandem Switching System (ETSS).

#### 5.2.1.1 Principles of Operation

Figure 5-1 illustrates the basic ideas behind DSDS, showing a 16 input 16 output digital space matrix which could be implemented on a 40-pin LSI chip. The output of the SR flip flops control the AND gates, either enabling a gate to pass a signal or disabling the gate to inhibit the signal. By enabling one gate in the first column any of the sixteen inputs can be connected to the first output. Switching is accomplished by setting or resetting a flip flop to the desired connection configuration.

Figure 5-2 presents an alternative implementation of a 16 x 16 space division switch. To simplify the discussion, it is assumed that the input channels are bit synchronized. During one bit time sixteen bits are multiplexed onto the interconnection, one bit from each of the sixteen inputs. The demultiplexer then directs these bits to the proper output where they are buffered to realign them. Switching is performed by controlling the demultiplexing order.

Both approaches to implementing DSDS as described above are constrained in the maximum number of inputs and outputs they can handle, but for different reasons. The size of the first approach is limited by the complexity of the hardware which grows as the product of the number of inputs and outputs. The size limitation in the second approach is due to the finite speed of the hardware which places an upper bound on the number of multiplex and demultiplex operations which can be performed during a single bit period. However, both approaches can take advantage of multistage network theory which provides for a reduction in the number of crosspoints required for a given number of inputs and outputs below that for a single stage matrix and thereby alleviates these size limitations. Clos [Reference 5-1] has described three, five, and seven stage non-blocking switching matrices made up of smaller matrices and



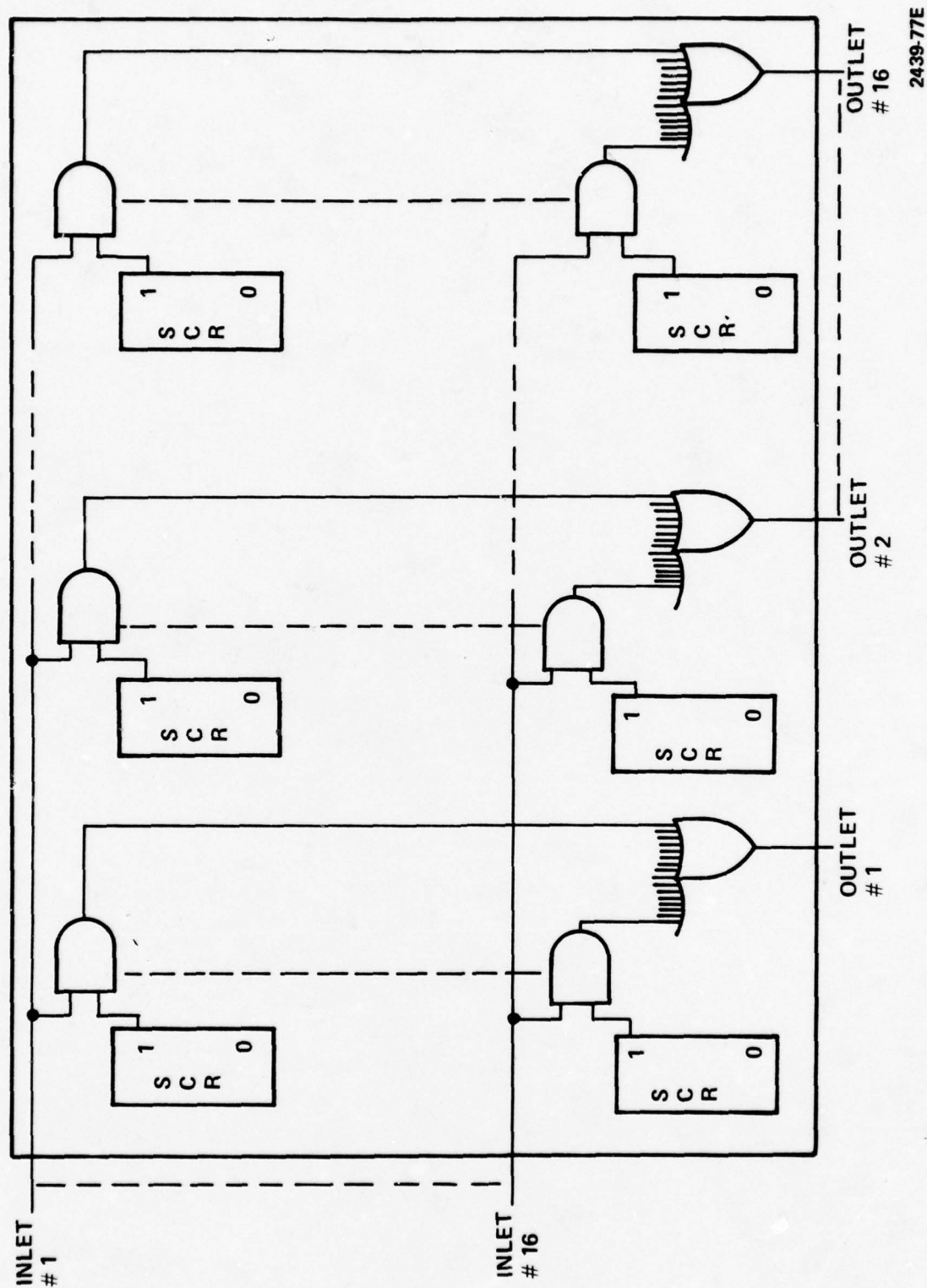
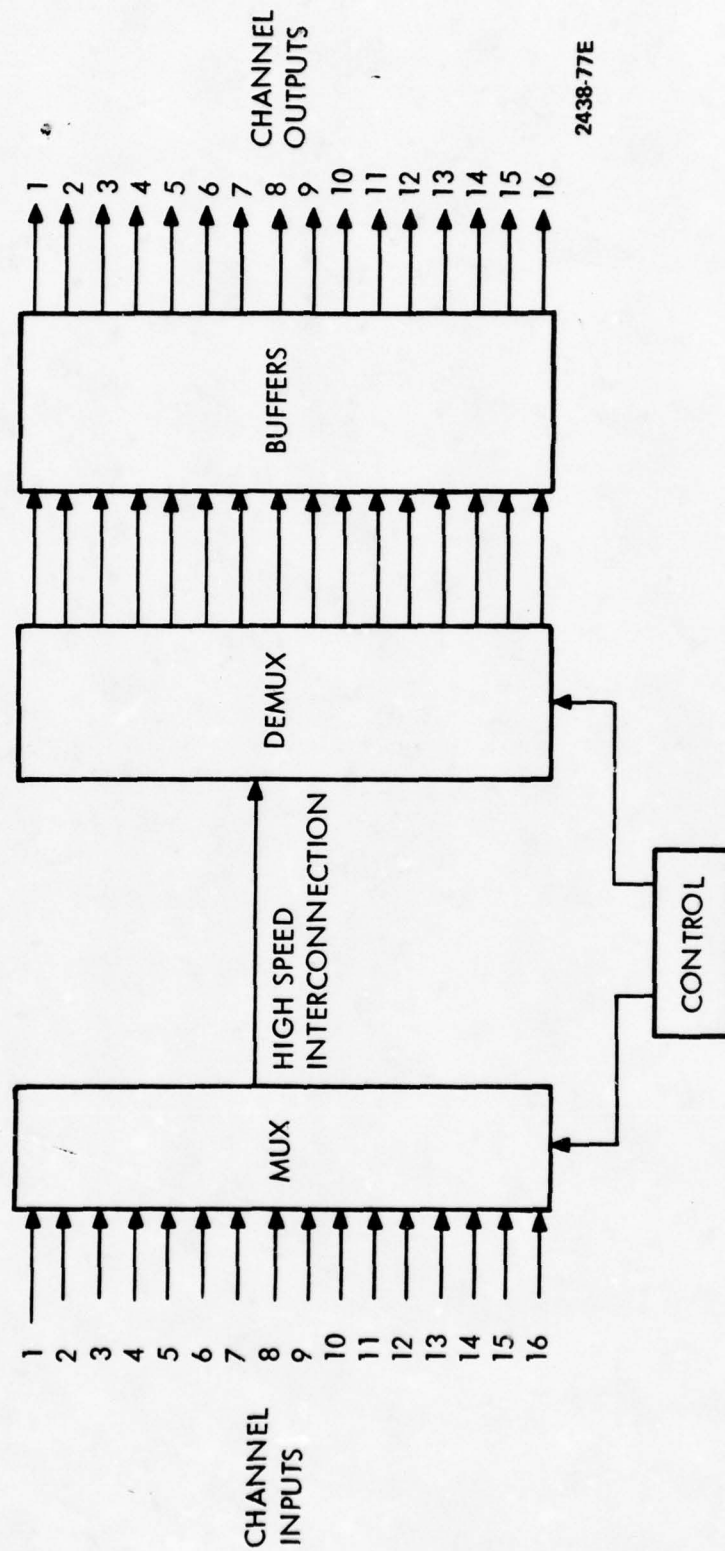


Figure 5-1. Digital Space Division Switching Matrix



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Figure 5-2. Alternative 16 Space Matrix

discussed techniques for determining the stage configurations to minimize the number of crosspoints. As an example, Figure 5-3 illustrates a 384 x 384 three-stage space matrix requiring a total of 48,128 crosspoints. A 384 x 384 single stage matrix would require 147,456 crosspoints.

#### 5.2.1.2 Baseline Configuration

Two considerations resulted in the selection of the mux/demux approach for the baseline configuration. Since for channel reassignment the device will interface T1 digital groups, for the first approach a demultiplexer is needed to break down the digital groups into their constituent channels prior to entering the space matrix and a multiplexer is required to recombine the channels back into digital groups after leaving the space matrix. The mux/demux approach uses multiplexers to perform the switching, so equipment savings can be realized in multi-stage matrices if the first and last stages use the mux/demux approach, as shown in Figure 5-4 a. and c. In addition the number of crosspoints that can be put on an IC is limited by the number of pins on the chip. Thus, the mux/demux approach requires fewer chips due to the multiplexing of the interconnection pin, allowing more crosspoints per IC.

A three-stage matrix is postulated for the baseline configuration because of the crosspoint reduction over a single stage and because of the computational complexity involved in configuring higher order matrices. Inputs and outputs are T1 digital groups at 1,544 Mb/s up to a maximum of 192. As mentioned previously, the input stage does not require a mux and the output stage does not require a demux because the inputs and outputs are themselves multiplexed. The maximum configuration would require 192 primary and tertiary stage units connected in a manner similar to Figure 5-3.

#### 5.2.2 Digital Time Division Switching (DTDS)

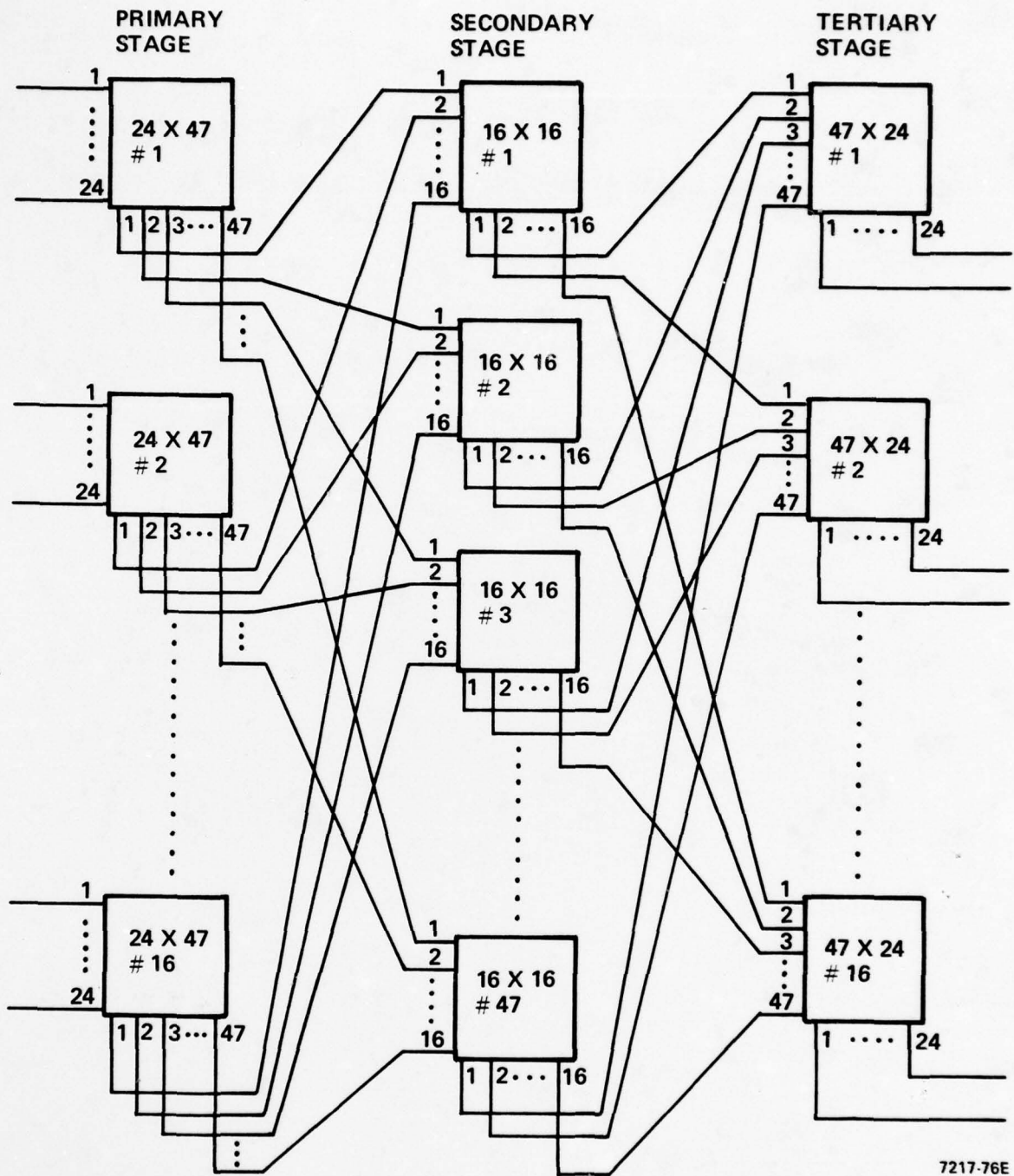
DTDS performs switching directly within the multiplexed bit streams without the need to break down the bit streams to the channel level as with space division switching. This technique is employed in several commercial and military units such as the AN/TTC-39 Circuit Switch, the AN/TSQ-111 (CNCE) Channel Reassignment Function, and the Collins Digital Tandem Switch (DTS).

##### 5.2.2.1 Principles of Operation

In a DTDS switch based on Random Access Memories (RAM), data is written sequentially into a RAM and read out in a different order. Figure 5-5 illustrates a basic time division matrix for three digital groups. During each bit time the following operations occur for each digital group:

- a. A data bit is written into a location, pointed to by the counter, in the digital group data memory.





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Figure 5-3. Example of 3-Stage Digital Space Division Switching

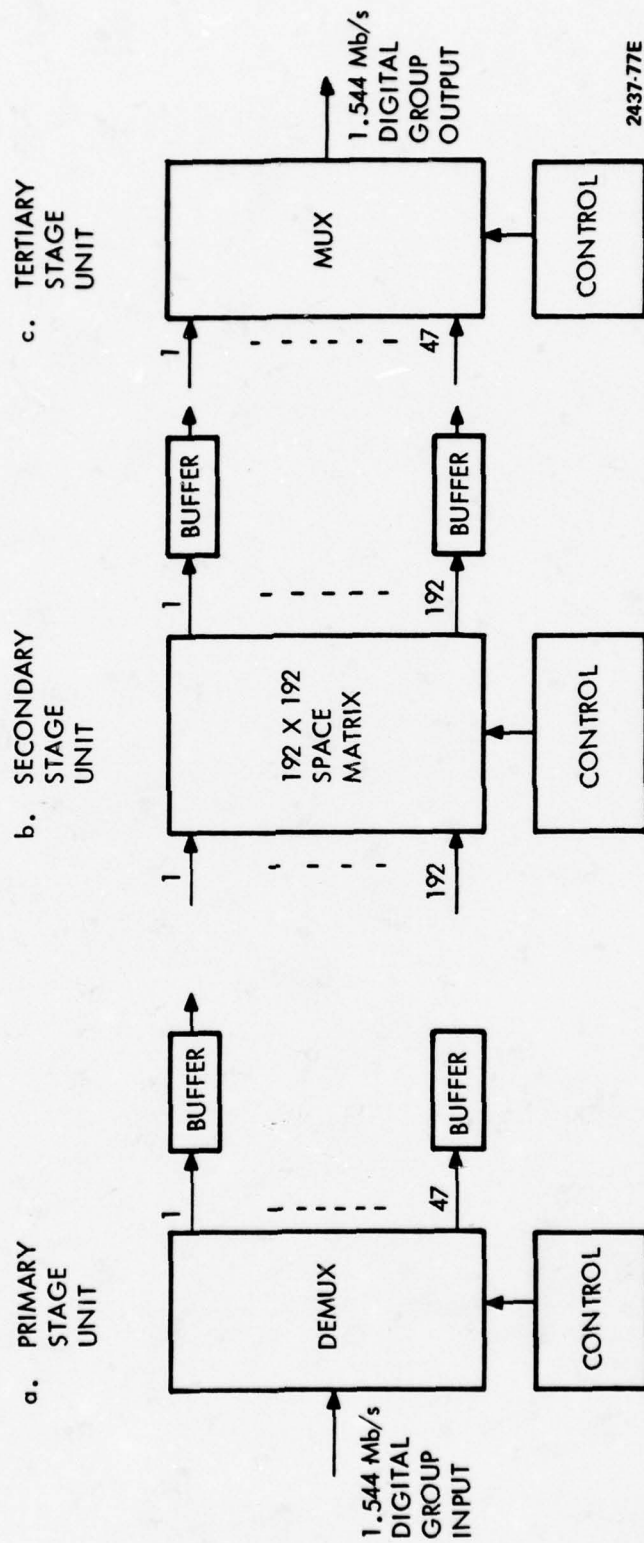
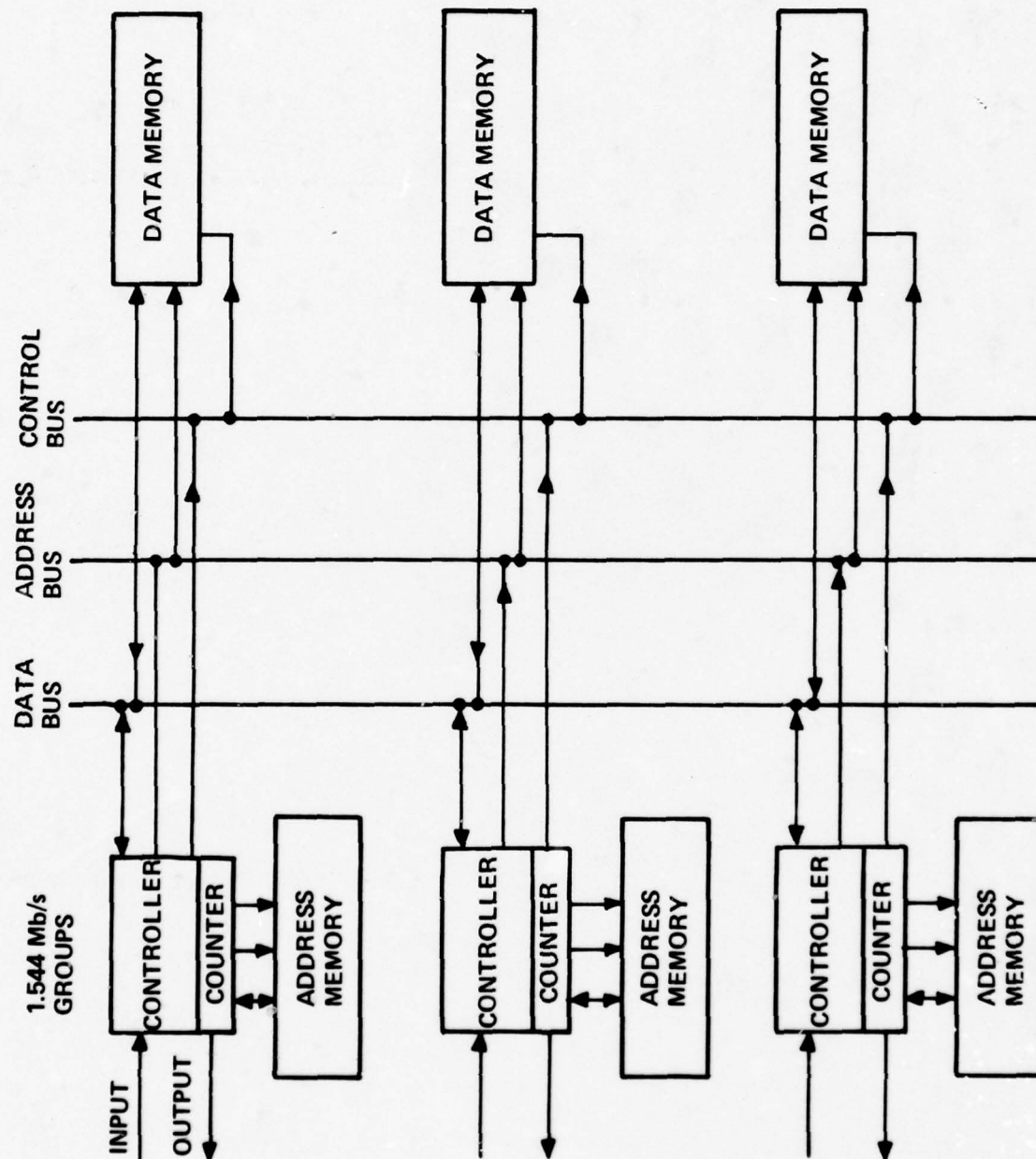


Figure 5-4. Baseline DSDS Configuration



ALL COUNTERS HOLD IDENTICAL VALUES

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Figure 5-5. Digital Time Division Switching



- b. A connection address is read from a location, pointed to by the counter, in the digital group address memory.
- c. A data bit is read from some location in one of the data memories, as pointed to by the connection address read in item b.
- d. The counter is incremented. If the end of the frame has been reached the counter is reset to begin a new frame.

Changing the connection addresses in the address memories controls the switching action of the DTDS matrix. Note that if two connection addresses are the same the addressed channel will be broadcast to two channels, but that the reverse (conferencing) cannot be accomplished by the DTDS matrix alone. Also, an alternative and functionally equivalent control algorithm is to write the data into the data memory according to the connection addresses and read it out sequentially. The steps for this technique, called write controlled DTDS (as opposed to read controlled DTDS), are:

- a. A connection address is read from a location, pointed to by the counter, in the digital group address memory.
- b. A data bit is written into some location in one of the data memories, as pointed to by the connection address read in item a.
- c. A data bit is read from a location, pointed to by the counter, in the digital group data memory.
- d. The counter is incremented or reset, as before.

Several other implementations of the DTDS exist. One uses cyclic memories such as shift registers instead of the RAMs used in the approach just described, but the control is similar. A different approach attaches keys to the incoming data according to its destination time slot and then sorts the data on the keys [Reference 5-2]. Neither implementation was considered further because both suffered from severe speed limitations and are not capable of handling the required maximum configuration of 192 digroups without excessive hardware costs being incurred.

In the RAM approach the data memories share a common bus which is multiplexed among them. For a given memory speed this results in a limit on the number of digital group data memories which can be attached to the bus. By adding multiple copies of the data memories and attaching them to multiple busses, the degree of multiplexing of each bus is reduced and hence more digital groups can be accommodated. Adding redundancy in this manner increases the parallelism but results in an undesirable growth characteristic. As the switch size grows, not only must more data memories be added to accommodate the new

groups, but more copies of the existing data memories must be added to increase the redundancy to the appropriate level. This results in the amount of RAM depending on the square of the number of digital groups.

Two modifications can be made to reduce the severity of this problem. One is to transfer more than one data bit at a time. For a fixed memory speed, this results in an increased memory and bus information bandwidth, allowing a lower level of redundancy. The second method is to perform the three memory accesses done for each data bit (i.e., one data memory write, one address memory read, and one data memory read) in parallel by providing two data memories. The operation for this approach is as follows for each digital group:

- a. In parallel write a data bit into one data memory according to the counter, read a connection address from the address memory according to the counter plus one, and read a data bit from the other data memory according to the connection address read in the previous bit time.
- b. Increment the counter. If the end of the frame has been reached, reset the counter and exchange the two data memories.

This method also reduces the redundancy problem. Figure 5-6 shows the memory constraint equation illustrating the effect of each technique on the level of redundancy. Method one affects  $n$  while method two affects  $I$ . For example, if  $C$ ,  $R$ ,  $I$ , and  $N$  are held constant and  $n$  is doubled (i.e., twice as many bits are now transferred per access), then the lower limit on  $D$  is halved. Similarly, with  $C$ ,  $R$ ,  $N$ , and  $n$  held constant using method two halves the limit on  $D$  when compared with not using method two.

#### 5.2.2.2 Baseline Configuration

The baseline configuration is a RAM based approach for the reasons mentioned previously. It is a read controlled matrix because this provides a broadcast capability not provided by a write controlled matrix. Both of the techniques discussed in the previous section for easing the severity of the redundancy problem (multiple bit transfers and dual data memories) are employed.

Figure 5-7 illustrates the baseline DTDS approach for 192 digital groups. Data bits are written into one data memory of each Dual Data Memory Module (DDMM) in a row via the input busses. Data bits are read out of the other data memory of each DDMM in a column under Output and Address Memory Module (OAMM) control, thereby accomplishing channel reassignment. The number of columns indicates the redundancy factor, not counting the last column which consists of hot standby modules for reliability purposes. Eight bits representing

$$D \geq \frac{CRNI}{n}$$

D = REDUNDANCY FACTOR (NUMBER OF COPIES OF EACH DATA MEMORY)

C = MEMORY CYCLE TIME (SECONDS)

R = DIGITAL GROUP DATA RATE (BITS / SECOND)

N = NUMBER OF DIGITAL GROUPS

I =  $\begin{cases} 1 & \text{IF METHOD 2* IS USED} \\ 2 & \text{IF METHOD 2 IS NOT USED} \end{cases}$

n = NUMBER OR BITS TRANSFERRED PER ACCESS

\* METHOD 2 - DATA MEMORY READ AND WRITE AND ADDRESS  
MEMORY READ ARE DONE IN PARALLEL BY  
USING DUAL DATA MEMORIES

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Figure 5-6. Memory Speed Equation



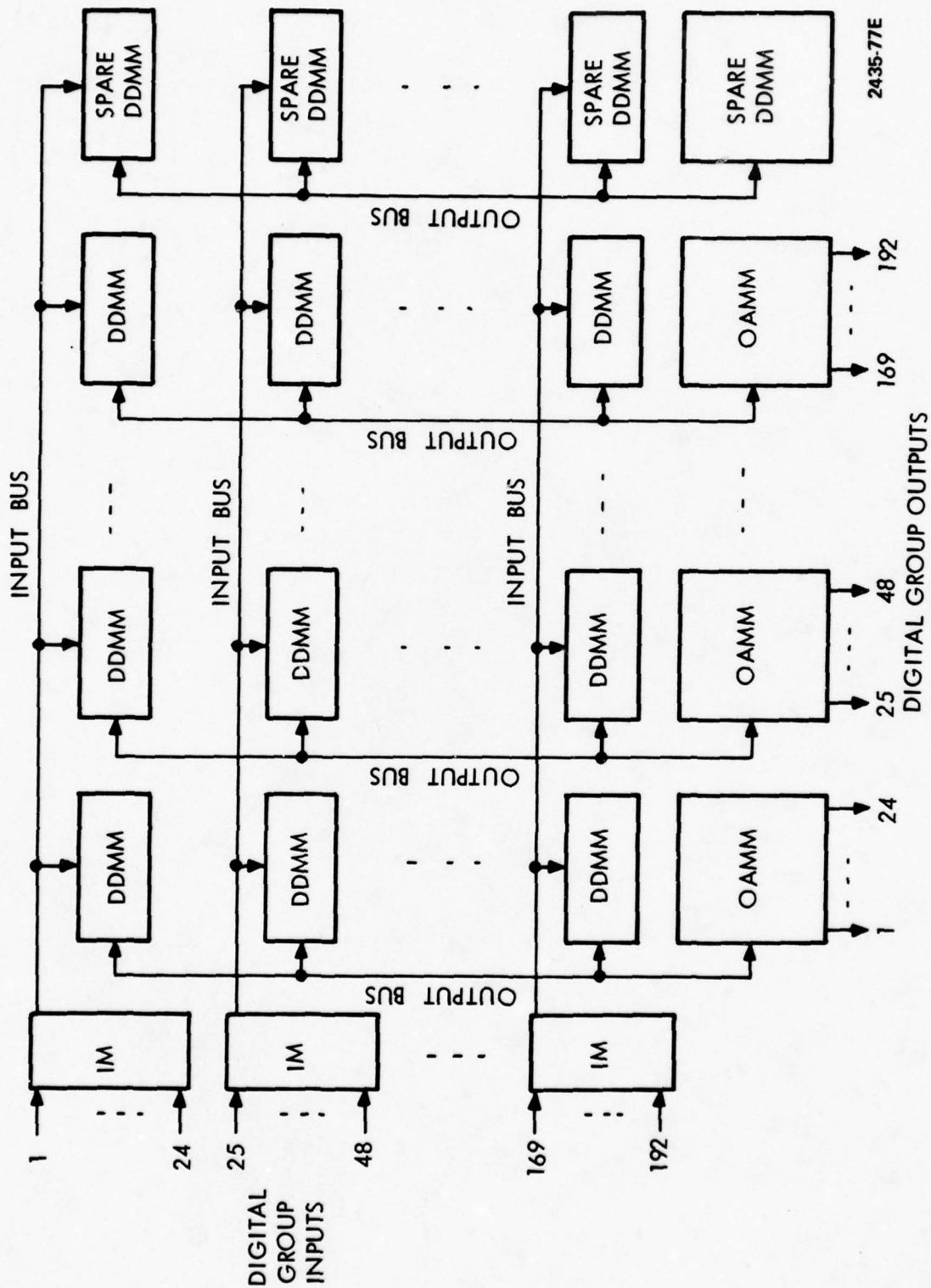


Figure 5-7. Baseline DTDS Configuration

one PCM channel sample are transferred per data memory access. A 200 ns cycle time memory was assumed, so for 192 digroups we have from Figure 5-6

$$D \geq \frac{(2 \times 10^7) (1.544 \times 10^6) (192) (1)}{8} = 7.41$$

and since D must be an integer  $D > 8$ . Using a redundancy of 8, each module must then handle  $192 \times 8 = 24$  digital groups, as shown in Figure 5-7. For smaller systems fewer columns and rows are required.

### 5.2.3 Software Directed Switching (SDS)

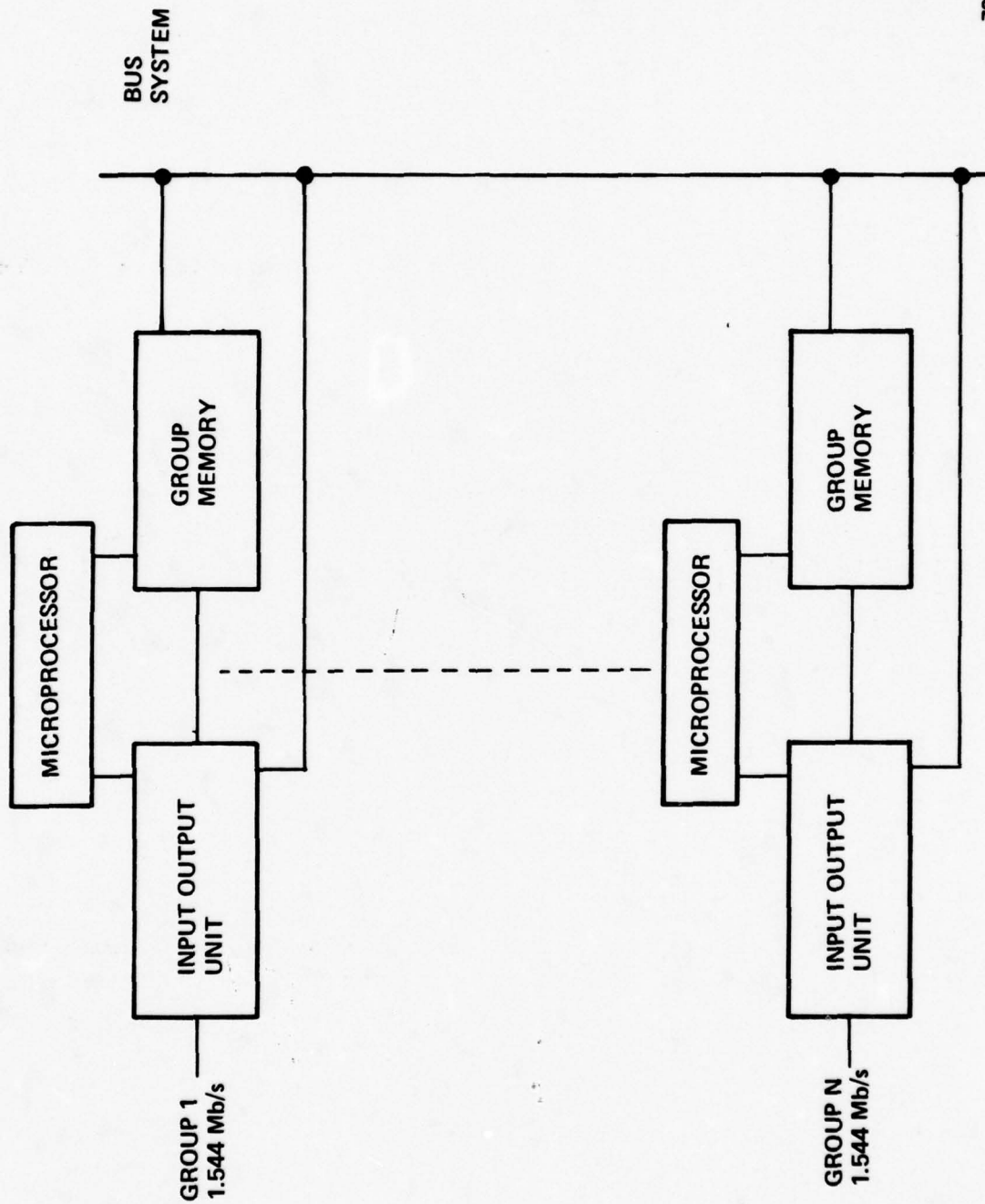
SDS is a relatively new approach to switching. A study performed at GTE Sylvania for DCA examined the feasibility and implementation considerations of SDS as applied to an integrated voice/data switching system using the SENET (Slotted Envelope Network) concept [Reference 5-3]. The SENET approach is somewhat similar to the TRAN M3200 PACUIT Switching System [Reference 5-4].

#### 5.2.3.1 Principles of Operation

The basic configuration is shown in Figure 5-8. Operation is similar to DTDS in that data bits are read into group memories and read out in a different order by the Input/Output Units under microprocessor control. The difference is that the microprocessors provide more flexibility in routing the data. By using data processing techniques SDS can switch channels with various data rates and route packets simultaneously.

The SENET concept utilizes a fixed size master frame divided into time slots. These slots are dynamically allocated among the voice and data traffic. Figure 5-9 shows the layout of the master frame. Part of the frame is allocated to start of frame indication and the rest is divided into a voice region, a data region, and a section representing unused capacity. The voice region always precedes the data region which in turn always precedes the unused capacity, but the size of each region is variable.

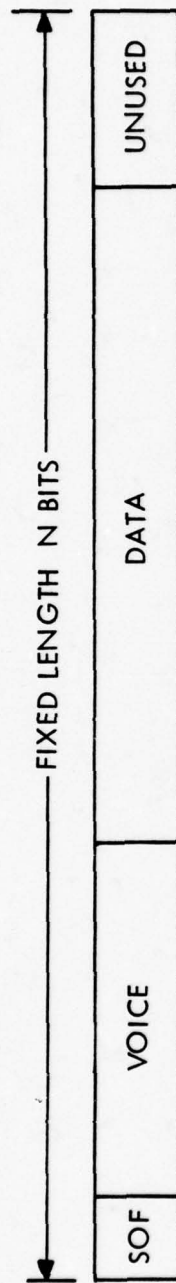
Figure 5-10(a) illustrates the layout of the voice region. Each channel occupies a certain number of slots, depending on its data rate. Figure 5-10(b) shows the layout of the data region. Packets of various sizes are packed contiguously in this region. Non-packetized data channels occupy slots in the voice region, while only packet- or message-oriented data occupies slots in the data region. Common Channel Interswitch Signaling (CCIS) information is transmitted in the data region. CCIS provides for the passing of control information between switches.



7201-76E

Figure 5-8. Software Directed Switching





2434-77E

SOF START OF FRAME INFORMATION

VOICE DIGITIZED VOICE AND NON-PACKETIZED DATA

DATA PACKETS AND MESSAGES

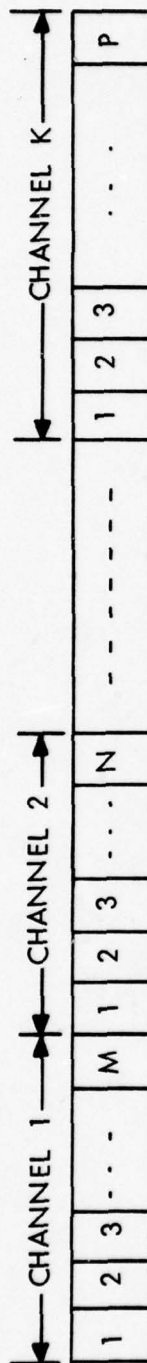
UNUSED REMAINING CAPACITY

SOF IS FIXED IN SIZE

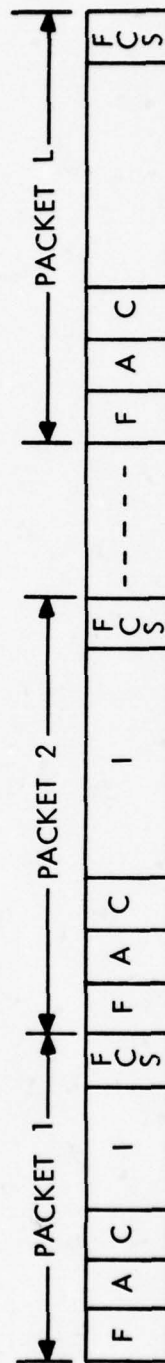
VOICE, DATA, UNUSED ARE VARIABLE IN SIZE

Figure 5-9. SENET Master Frame Structure

## A) VOICE REGION



## B) DATA REGION



F = FLAG

A = ADDRESS FIELD

C = CONTROL FIELD

I = INFORMATION FIELD

FCS = FRAME CHECK SEQUENCE

2433-77E

Figure 5-10. SENET Region Structures

The Input/Output Units perform the actual transfers between the group memories and the digital groups because these transfers occur too rapidly for most current microprocessors to handle. This frees the microprocessors to perform a supervisory role, controlling the actions of the Input/Output Units. Common functions, such as the man/machine interface, are handled by the Common Control Unit attached to the bus system.

Since the digital groups share a common bus system as in the basic DTDS approach, SDS has similar speed limitations. As with DTDS the techniques of redundancy, dual data memories, and multiple bit transfers can be used to overcome these problems and the memory speed equation is the same.

#### 5.2.3.2 Baseline Configuration

The SDS baseline configuration is shown in Figure 5-11 for 48 digital groups. The same timing considerations mentioned for DTDS apply here and result in a maximum of 24 digital groups sharing one bus. For 48 digital groups there are two busses with the first 24 digroups attached to the first bus and the second 24 digital groups attached to the second bus. Each digital group has two dual data memories, one attached to each bus. An Input/Output Unit writes data into one-half of its associated dual data memories and reads data using the bus system to which it is attached. As with DTDS, 200 ns memory and byte transfers are used. Expanding to larger systems entails adding data memories and expanding the bus system. An additional unit is added to each bus as a hot standby. For the maximum configuration (192 digital groups) there are eight busses.

#### 5.2.4 Combined Space-Time Switching (CSTS)

CSTS is a hybrid approach using both space division and time division matrices in a multi-stage array similar to the Clos networks mentioned previously. This technique is used in large digital switches such as the AT&T No. 4 ESS [Reference 5-5].

##### 5.2.4.1 Principles of Operation

CSTS utilizes multiple space and time division switches in a staged array to reduce the amount of hardware required when compared with DTDS. The notation used to describe the order of the stages consists of a string of T's and S's. For example, a time-space-time matrix is denoted as TST.

Figure 5-12 shows a TST matrix which can handle  $N_n$  digital groups. Each time division module handles  $n$  digital groups and there are  $N$  modules in both the primary and tertiary stages. The secondary stage space matrix is therefore  $N_n$  by  $N_n$ . The operation of the TST switch can be most easily understood by working backwards from the output. The tertiary stage time division modules receive data bits from the secondary stage and organize them in the proper order for transmission on the appropriate digital group output. Each tertiary



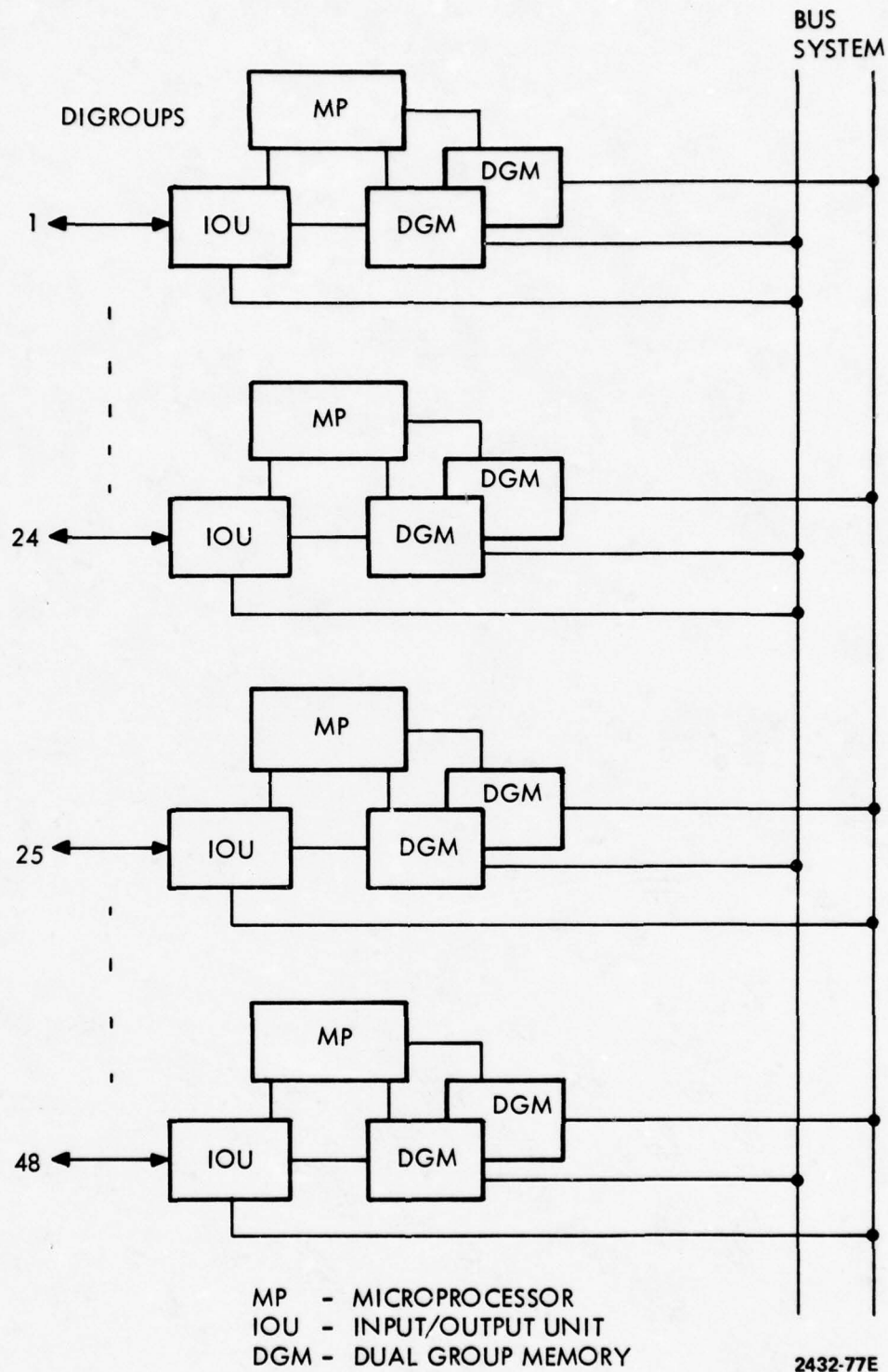
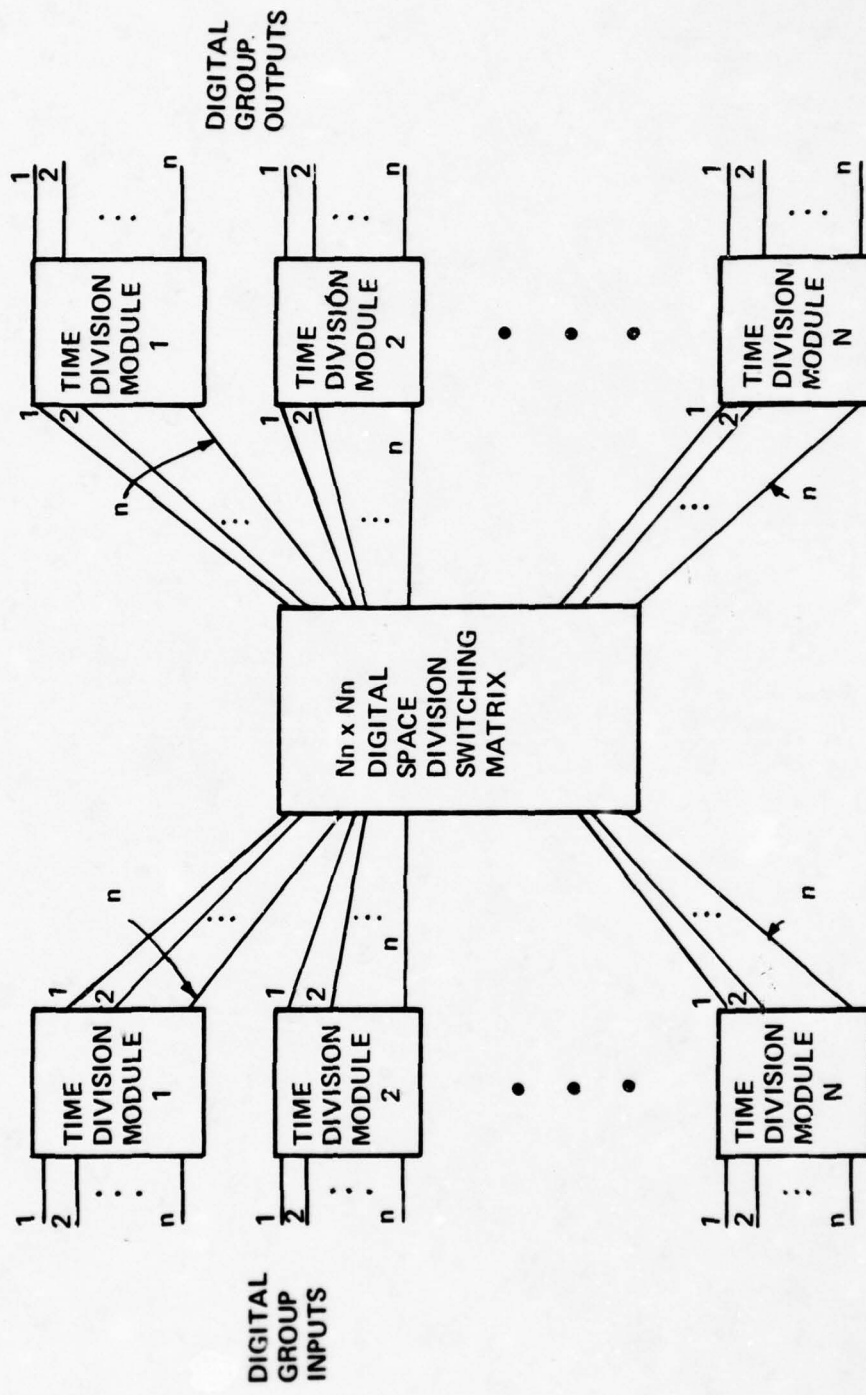


Figure 5-11. Baseline SDS Configuration



7193-76E

Figure 5-12. Combined Space-Time Switching

module organizes the output data for  $n$  digital groups. The space matrix which makes up the secondary stage receives data bits from the  $N$  primary modules and routes them to the proper tertiary modules. It changes its connections every bit time to properly route the data in the digital group. The primary stage modules organize the input data so that the secondary stage can route it. The primary stage handles the case where  $m > n$  channels arrive simultaneously and are to be routed to the same tertiary stage module. Since the tertiary module has only  $n$  inputs the primary modules must spread out the  $m$  data bits over time so that no more than  $n$  occur simultaneously.

There are many alternative configurations to TST for CSTS matrices. STS differs in operation from TST in that there is only one time stage. This means that any repositioning in time of data bits must be done in the secondary stage as opposed to TST where most, but not all, of the temporal switching is performed in the tertiary stage. Matrices with more than three stages can be built by expanding the center stage of a TST or STS matrix. For example, if the secondary stage of TST is a three-stage Clos network we have a TSSST matrix. Using TST as the center stage in an STS matrix yields an STSTS matrix. Other configurations are also possible such as the No. 4 ESS which uses a TSSSST matrix.

CSTS is advantageous for use in large switches because of its improved growth characteristics when compared with DTDS. Since each time division module is fixed in size and the switch grows by adding modules, CSTS does not suffer from the redundancy problems of DTDS, thus giving it nearly linear growth characteristics as opposed to geometric for DTDS. Note that the time division modules can be optimized as discussed in Section 5.2.2.1 and could also be implemented using SDS instead of DTDS.

#### 5.2.4.2 Baseline Configuration

The baseline configuration for CSTS is as shown in Figure 5-13 for the maximum size of 192 digital groups. Each time division module is a DTDS baseline configuration matrix handling 24 digroups as described in Section 5.2.2.2 but does not include a spare dual data memory module nor a spare output and address memory module. A spare time division module is provided as shown for both the primary and tertiary stages in a hot standby mode. The secondary stage space matrix is a 192 x 192 DSDS matrix as used on the DSDS baseline configuration center stage, described in Section 5.2.1.2, with the addition of a controller to enable it to perform the data routing function previously described. The minimum system would include one active primary module, one active tertiary module, one spare primary module, one spare tertiary module, and the secondary stage matrix and controller.



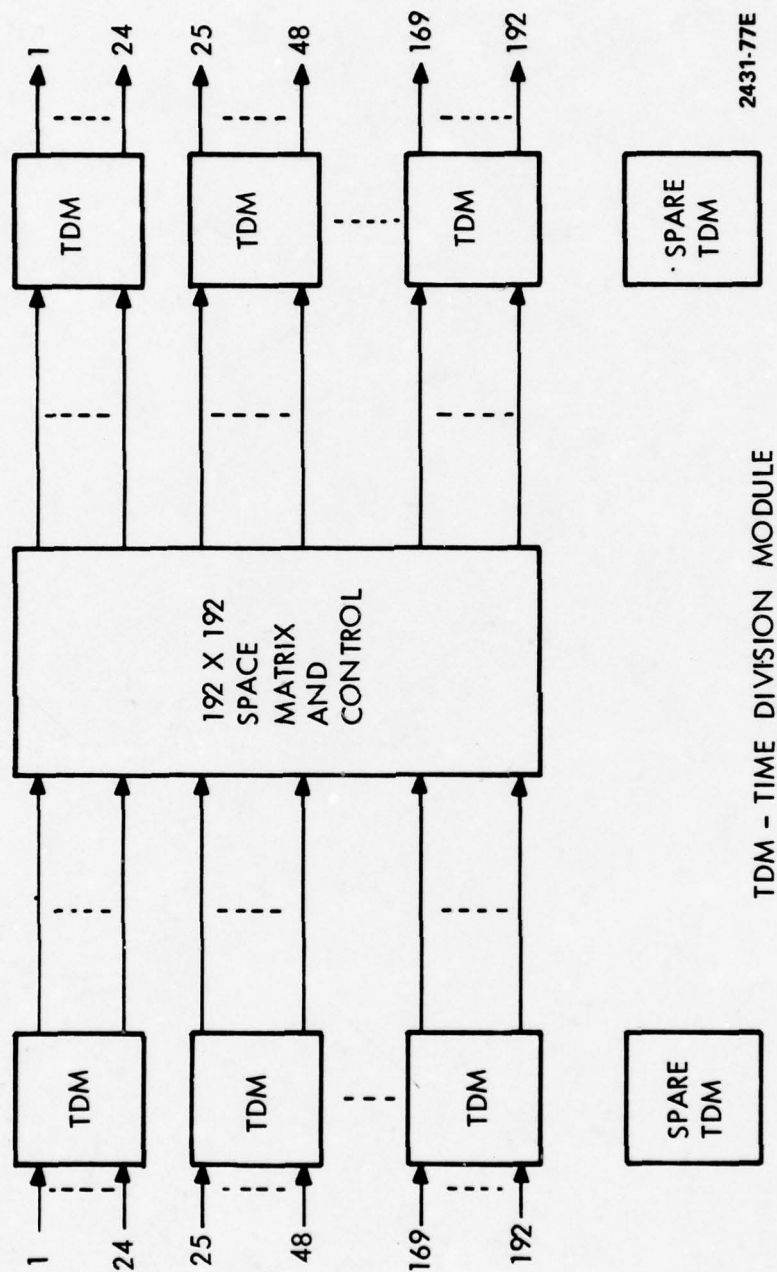


Figure 5-13. Baseline CSTS Configuration

### 5.3 ANALYSIS AND TECHNIQUE SELECTION

This section presents the results of the evaluation phase of the channel reassignment technique selection. The four candidate techniques were compared using each of the five evaluation criteria and the results are shown in Tables 5-4, 5-5, 5-6, 5-7, 5-8 and 5-9. For each candidate and criteria, an absolute rating on a scale from one to ten is generated and then multiplied by the weighting factor for that criteria to yield the weighted rating, also from one to ten. A relative ranking based on the weighted ratings is determined for each criteria and for the total sum.

#### 5.3.1 Equipment Cost

The relative equipment cost for the four candidate techniques are shown in Table 5-3 for various switch sizes up to the maximum of 192 digroups with the cost of a 24 digroup DTDS matrix defined to be 1.0. The cost estimates are based on the number and type of ICs and the number of boards required.

TABLE 5-3. RELATIVE COSTS, DTDS (24) = 1.0

NUMBER OF DIGROUPS	DSDS	DTDS	SDS	CSTS
24	4.8	1.0	3.8	2.7
48	10.0	2.0	7.8	3.7
72	15.0	3.3	11.8	4.7
96	19.8	5.0	16.0	5.7
120	24.8	7.0	20.3	6.7
144	29.8	9.3	24.7	7.7
168	34.3	12.0	29.2	8.7
192	39.1	15.0	33.9	9.7

It can be seen that DSDS is the most costly technique in terms of equipment cost for all switching matrix sizes, followed by SDS. The costs for these two techniques grow nearly linearly with the number of digital groups. CSTS cost is also linear and is less than both DSDS and SDS for all sizes. DTDS cost does not grow linearly but instead grows geometrically with the number of digroups. This results in a crossing of the size/cost curves of DTDS and CSTS between 96 and 120 digital groups. Below 96 digital groups DTDS has the lowest

equipment cost while above 96 digital groups CSTS has the lowest equipment cost. Since most sites would require a switching matrix to handle less than 80 digital groups DTDS is rated higher than CSTS. The ratings are shown in Table 5-4.

TABLE 5-4. EQUIPMENT COST RATINGS  
WEIGHTING FACTOR = 1.0

	ABSOLUTE RATING	WEIGHTED RATING	RELATIVE RANKING
DSDS	4	4.0	4
DTDS	9	9.0	1
SDS	5	5.0	3
CSTS	8	8.0	2

#### 5.3.2 R/M/A

The ratings of the four techniques for reliability, maintainability and availability are presented in Table 5-5. Reliability is estimated using the number of ICs and the number of pins per IC to calculate the total number of pins. Maintainability estimates are based on qualitative assessments of the ease of repair, which is affected by any automatic fault analysis which can be performed. Availability is determined by the above factors and by automatic fault correction capabilities, if any.

TABLE 5-5. R/M/A RATINGS  
WEIGHTING FACTOR = 0.9

	ABSOLUTE RATING	WEIGHTED RATING	RELATIVE RANKING
DSDS	4	3.6	4
DTDS	8	7.2	1
SDS	8	7.2	1
CSTS	8	7.2	1



The results are listed in Table 5-5. DSDS was downgraded severely for several reasons. It has the worst reliability estimate of the four techniques because of the large number of ICs of low to medium complexity which results from the pin limitation discussed in Section 5.2.1.1. The equipment cost of providing Built-In Test Equipment (BITE) to isolate faults is high because of the large number of switch modules involved. Adding more ICs to perform BITE further reduces reliability. Automatic standby switching is also expensive because of the large number of modules and because of the complexity of the inter-stage connections. Finally, three different card types must be stocked as spares.

DTDS, SDS, and CSTS were all rated well above DSDS. Both DTDS and CSTS have good reliability estimates because they both utilize complex LSI chips which reduces the pin count. SDS also uses LSI, but requires many more packages than DTDS or CSTS, although its reliability is still above DSDS. All three are amenable to BITE because of the fewer number of modules. BITE is most costly for SDS because it has more modules than DTDS or CSTS, but its distributed processing power can provide a high degree of rapid fault isolation. Additionally, SDS has only one card type while both DTDS and CSTS have three. Availability is equally good for these three techniques as all provide hot standby modules with SDS having a slight advantage due to its rapid fault isolation capability.

### 5.3.3 Control Complexity

Control complexity is evaluated qualitatively for the four candidate techniques. The control algorithms are considered but no control implementations are analyzed because each algorithm could be realized in a variety of ways in hardware, software, or some combination.

In Table 5-6 SDS is rated lowest in control complexity. This is due to the complexity of coordinating all the digital group microprocessors and the extensive common control and interprocessor communication required. In addition, there is substantial software in each microprocessor to handle the SENET concept, but this is not required for the channel reassignment application and thus was not considered. Since the degree of flexibility and processing power provided by SDS also is not required by this application, the control complexity necessary to support this approach resulted in its poor rating.

The other three techniques have very limited distributed control. This greatly reduces the coordination and communication complexity required. The algorithms for these three are similar in many respects with one major difference. Both CSTS and DSDS are multi-stage switches which require additional control effort beyond that required for the single stage of DTDS. The algorithms for the CSTS and DSDS are very similar, as both are three-stage matrices with the first two stages routing data to the proper tertiary stage modules for output. The CSTS primary stage spreads data bits out over time to

allow routing by the secondary stage while the DSDS primary stage spreads data bits out over space. Conceptually the operations are the same. As a consequence, CSTS and DSDS were rated the same and above SDS but below DTDS.

TABLE 5-6. CONTROL COMPLEXITY RATINGS  
WEIGHTING FACTOR = 0.7

	ABSOLUTE RATING	WEIGHTED RATING	RELATIVE RANKING
DSDS	7	4.9	2
DTDS	9	6.3	1
SDS	5	3.5	4
CSTS	7	4.9	2

#### 5.3.4 Modularity

The modularity comparison used a qualitative estimate of the ease of changing the size of a switch while it is in use and a quantitative estimate of the amount of equipment which is unused for switch sizes other than multiples of the switch modularity. It is desirable to be able to configure a switch as closely as possible to the number of digroups it will handle and to be able to add or delete digital groups without affecting the operation of the rest of the switch.

Table 5-7 shows that SDS was rated very high. It is capable of being configured exactly to the number of digroups and its size can be changed by inserting or deleting cards without affecting the rest of the system. Both DTDS and CSTS can be reconfigured while running but the increment is 24 digroups so that on the average a switch will be 12 digroups too big (assuming all switch sizes are equally probable). DSDS is also configured in multiples of 24 but changing the switch size while operating entails changes in the inter-stage connections which means that communication on other digroups will be interrupted during the switch modification.

TABLE 5-7. MODULARITY RATINGS  
WEIGHTING FACTOR = 0.5

	ABSOLUTE RATING	WEIGHTED RATING	RELATIVE RANKING
DSDS	6	3.0	4
DTDS	8	4.0	2
SDS	10	5.0	1
CSTS	8	4.0	2

### 5.3.5 Size and Power

The size estimates are based on the number of boards required and the power estimates are based on the number of ICs and their power consumption. These estimates closely follow the equipment cost and reliability factors obtained previously. This is true for two reasons. First, the printed wiring boards and the cost to place ICs on them represent a major portion of the total equipment cost. Second, the more boards required, the more ICs required which in turn means more pins and hence poorer reliability.

Table 5-8 presents the results of this comparison. As expected, DSDS and SDS are the lowest rated techniques with SDS requiring 3 to 4 times the number of boards and power as DTDS while DSDS requires 6 to 10 times the number of boards and power (depending on switch size). Also as expected, DTDS requires fewer boards and less power than CSTS for less than 96 digital groups but more than CSTS for more than 96 digroups. Again, since most switches will handle less than 80 digroups DTDS was rated higher than CSTS.

TABLE 5-8. SIZE AND POWER RATINGS  
WEIGHTING FACTOR = 0.3

	ABSOLUTE RATING	WEIGHTED RATING	RELATIVE RANKING
DSDS	4	1.2	4
DTDS	9	2.7	1
SDS	5	1.5	3
CSTS	8	2.4	2



### 5.3.6 Technique Selection

Table 5-9 sums the ratings of the four candidate techniques over the five evaluation criteria. As a result, DTDS is the technique selected to implement the channel reassignment function. DTDS has low equipment costs, good R/M/A, simple control algorithms, good modularity, small size, and low power. CSTS has slightly higher equipment costs, size requirements, and power consumption, and has a more complex control algorithm. SDS has better R/M/A and modularity but it and DSDS have much higher equipment costs and size and power requirements. SDS has the most complex control algorithms while DSDS has the poorest R/M/A and modularity.

TABLE 5-9. OVERALL RATINGS

	ABSOLUTE RATING	WEIGHTED RATING	RELATIVE RANKING
DSDS	25	16.7	4
DTDS	43	29.2	1
SDS	32	22.2	3
CSTS	39	26.5	2

### 5.4 16/32 kb/s TECHNIQUE SELECTION

The analysis discussed in Section 5.3 is extrapolated to determine the optimal switching technique to handle T1-type digital groups at 1.544 Mb/s consisting of bit interleaved 16 and 32 kb/s CVSD channels as opposed to byte interleaved 64 kb/s PCM channels. The impact of this different format on the baseline configurations is examined and the resulting perturbations of the ratings are analyzed to determine if the relative rankings of the four techniques have changed.

#### 5.4.1 Baseline Configuration Modifications

In Section 4 it was determined that the 16/32 kb/s channel reassignment function would handle up to a maximum of 27 T1 digital groups. The two bits from a 16 kb/s channel which appear in a T1 frame period should be placed contiguously in the T1 frame in order to provide maximum usage of the transmission facilities. This means that each 16 kb/s channel should be treated as two 8-kb/s channels in order for the switching matrix to be able to pack the two bits together, since the bits are not contiguous when they come into the reassignment

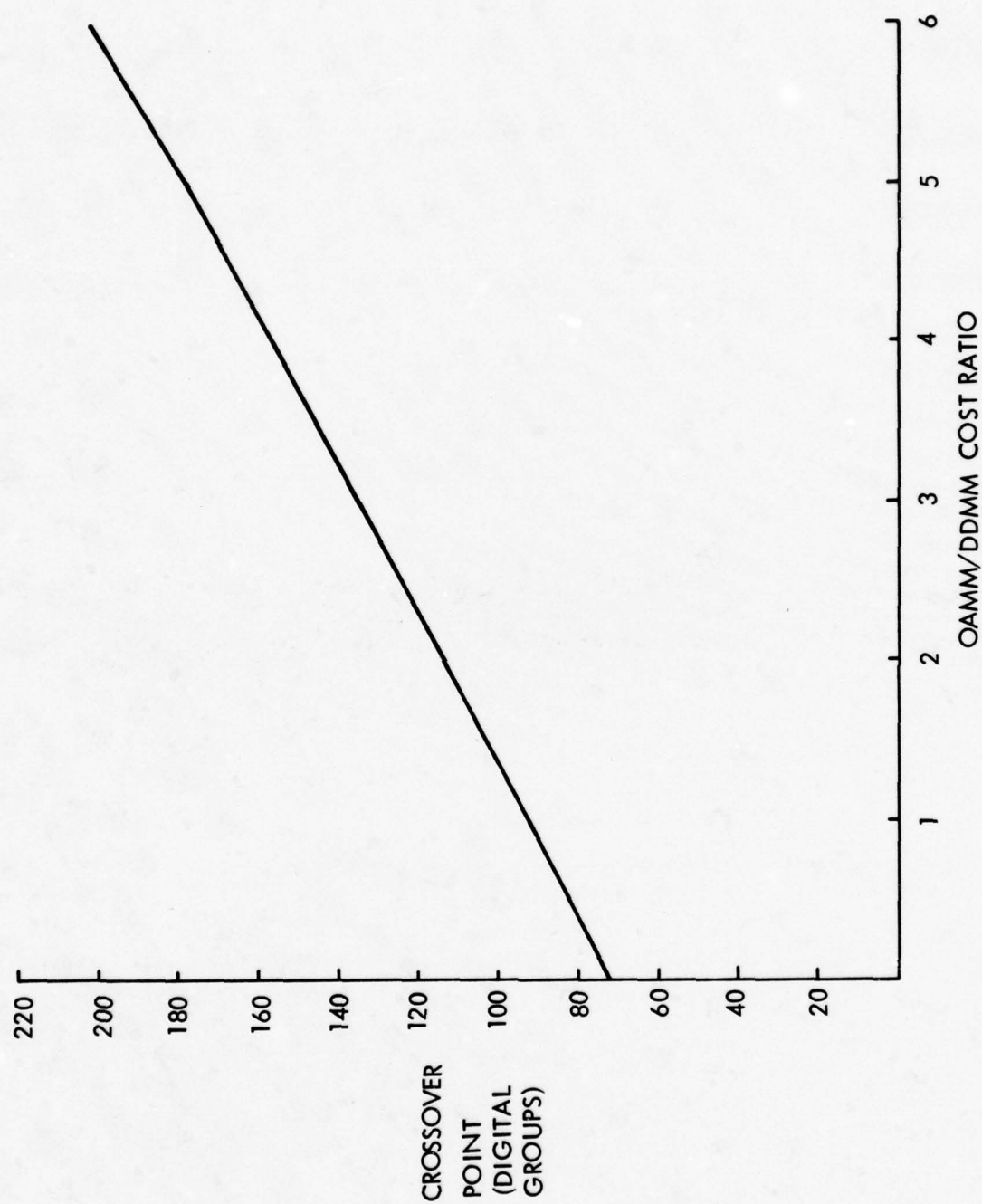
device from AUTOSEVOCOM II or TRI-TAC. Hence, the maximum case results in  $27 \times 192 = 5184$  8-kb/s channels as opposed to  $192 \times 24 = 4608$  channels for the maximum 64 kb/s PCM case. Also important is the fact that the channels are bit interleaved instead of byte interleaved. To convert a PCM channel to eight-bit parallel in order to permit multiple-bit accesses to the data memory, as described in Section 5.2.2.1, it is only necessary to put it through an eight-bit serial-to-parallel converter. For bit interleaved channels, however, the eight bits are not contiguous in the bit stream but are contained in eight different minor frames. Hence, buffering is necessary to collect the eight bits together from all the channels so that it can be converted to parallel.

The two differences just mentioned affect the size and configurations of the four techniques. DSDS must now be larger to handle the increase in the number of channels. DTDS, SDS, and CSTS handle fewer digital groups but each digroup now requires a larger address memory because there are eight times as many channels per digital group. Also, it is not cost effective to convert the bit interleaved digital groups to byte interleaved digital groups prior to entering the switching matrix so that byte transfers, as used in the 64 kb/s case, are not feasible. This means that a time module can only handle  $24 \div 8 = 3$  digital groups.

#### 5.4.2 Evaluation Criteria Impact

These modifications have several effects on the ratings for all the evaluation criteria except control complexity. The increase in channels results in a proportional increase in the equipment cost for DSDS with a corresponding increase in the size and power requirements and a decrease in R/M/A. The equipment costs, size and power, and reliability of DTDS, SDS, and the time modules of CSTS are affected to different degrees. The format change results in less data memory but more address memory per digital group and an output controller (or microprocessor for SDS) now handles only three digital groups. SDS is affected least because its controllers only handled one digital group apiece in the 64 kb/s case so the change is only in the sizes of the address and data memories. DTDS and CSTS, on the other hand, now require more controllers to handle the same number of digroups. However, DTDS still has lower equipment costs than CSTS because of its lower percentage of hardware associated with output controllers and address memory than CSTS. Figure 5-14 shows the cost curve cross over point in digital groups for DTDS and CSTS versus the ratio of the Output and Address Memory Module (OAMM) cost to the Dual Data Memory Module (DDMM) cost. Since the 16/32 kb/s case results in a higher OAMM/DDMM cost ratio, DTDS will still have better equipment cost, reliability, and size and power ratings than CSTS.

It remains to be determined if SDS will rank higher than DTDS. It was shown above that both have increased equipment costs; however, DTDS increases by about a factor of four while SDS increases by a factor of two. From Table 5-3 it is apparent that after the costs have been adjusted DTDS is still lower than SDS. Additionally, DTDS



OAMM - OUTPUT AND ADDRESS MEMORY MODULE  
 DDMM - DUAL DATA MEMORY MODULE

2430-77E

Figure 5-14. DTDS-CSTS Cost Crossover



now is much more modular than before, reducing the advantage SDS possessed in this area. From this extrapolation it is apparent that DTDS is the preferred approach for reassignment of 16/32 kb/s CVSD channels as well as for reassignment of 64 kb/s PCM channels.

## SECTION 6

### DNC IMPLEMENTATION

This section presents the chosen implementation for Digital Network Control (DNC) and discusses the rationale behind the selection of this approach. The requirements and applications in Sections 3 and 4 and the results of Section 5 provide input to the selection decision. Section 7 provides a more detailed description of the design including hardware, software, and reliability.

Section 6 is divided into two parts. It begins with an examination of the applicability of existing hardware and an overview of the selected implementation of DNC. The hardware operation and control of the Digital Control Element (DCE) are discussed as they apply to DNC. The second part of Section 6 presents the algorithms used for DNC. Operation scenarios are used to describe the manner in which the DCE is controlled to perform DNC.

#### 6.1 EXISTING HARDWARE

Section 5 examined four techniques for implementing a channel reassignment capability and selected digital time division switching as the preferred alternative. This subsection evaluates existing hardware employing this technique to determine if this hardware can satisfy the requirements of DNC in a cost-effective manner. The alternative to the use of existing hardware is to design hardware expressly for DNC using digital time division switching. As discussed in Sections 4.2.2 and 5.4, the reassignment of 64 kb/s and AII/TRI-TAC channels are treated separately.

##### 6.1.1 64 kb/s Channel Reassignment

Several commercial digital switches perform reassignment of 64 kb/s channels within T1 digital groups, such as the Collins Digital Tandem Switch. The major drawback to the use of commercial switches for DNC is that they provide more capabilities than are needed. Switches not designed as tandem switches provide PCM equipment to terminate analog loops, a function performed by the TD-1192. All switches provide signaling, supervision, routing, and service functions, such as call-forwarding, which are not required for DNC. As a result, the cost of the hardware and software is much greater than is necessary to perform the channel reassignment function of DNC. Also, the size of the hardware and the complexity of the software are greater than necessary. A possible solution is to utilize just the switching matrix portion of a switch and design a processor and software to enable it to perform DNC channel reassignment. However, a detailed analysis of the switching matrices of commercial switches would be necessary to determine if any could be "unbundled" from the rest of the hardware in a simple and cost-effective manner, a task which is beyond the scope of this study. Therefore, it is recommended that this study proceed with the design of a channel reassignment device, henceforth termed the Digital Control Element (DCE) to perform DNC functions for 64-kb/s channels within T1 digital groups.

### 6.1.2 AUTOSEVOCOM II/TRI-TAC Channel Reassignment

Several military devices perform digital time division switching of 16 and 32 kb/s channels, such as the AN/TTC-39 Circuit Switch and the AN/TSQ-111 (CNCE) Channel Reassignment Function (CRF). The AN/TTC-39 suffers from the disadvantages discussed in Section 6.1.1 because it is a complete switch; hence, it is not discussed further. The CRF, on the other hand, is not a full switch but rather is just the switching matrix and associated support equipment, such as frame alignment and synchronization hardware. It does not perform signalling, supervision, and other switch-related functions which are not required for DNC. Hence, with the addition of a processor and software to control it, the CRF is a potential candidate for the DNC "B" function (see Section 4.2.3).

The CRF would be deployed in a manner similar to that shown in Figure 3-6. The CRF would replace the channel patch panels, subchannel patch panels, subchannel muxes, and some, possibly all, of the DGM muxes. It also would replace the channel submux which combines seven 16 kb/s channels into a 128 kb/s group, but cannot replace the submux which combines three 16 kb/s channels into a 64 kb/s group, because 64 kb/s is not a TRI-TAC group rate. As shown, the CRF interfaces to the channel side of TD-1192s because it cannot handle T1 digital groups or any of the various TD-1193 super group rates.

The configuration described above has several serious drawbacks because the CRF would be located at the channel level in the DCS multiplex hierarchy. Since it interfaces with the TD-1192 it is only compatible at the channel rate of 16 kb/s (with a resulting overhead of 48 kb/s), at 64 kb/s via a channel submux (an overhead of 16 kb/s), or at the group rates of 128, 256, and 512 kb/s. DNC hardware at the group level can provide a much broader spectrum of compatible rates between the DCS transmission backbone and TRI-TAC/AII. Inefficiency is also present where an overhead channel in a TRI-TAC/AII group which passes through the DCS transmission backbone is used solely for framing purposes. An example would be a group of AII users not located at a switch site. Their channels are muxed together to be sent to the switch via the DCS. With the CRF, this overhead channel must be carried along through the DCS in order to properly break out the channels at their destinations. DNC "B" hardware at the group level, however, can provide a Digital Multiplex Applique function which uses the framing of the T1 digital group to identify the 16/32 kb/s channels; hence, no framing overhead channel is required.

Another problem is the fact that the framing pattern for TRI-TAC groups at the 32 kb/s digitalization rate (1010...) has the same format and frequency as the T1 framing pattern. If such a group were inputted into a TD-1192 at 128, 256, or 512 kb/s, the resulting T1 digital group would contain two identical framing patterns - one real and one false. This could result in the downstream TD-1192 synchronizing on the false framing pattern thereby causing an



unalarmed loss of service. Hence the TRI-TAC framing channel must be altered prior to input to the TD-1192 so that this interference does not occur. The CRF requires, as discussed above, that some framing be used so that the 32 kb/s channels can be correctly broken out. The suppressed framing pattern (1100...) cannot be used because type three groups already contain suppressed framing patterns. This means that a third framing pattern must be devised. DNC "B" hardware at the group level does not require that this framing pattern be passed through the DCS in order to correctly break out the 32 kb/s channels. Hence the interfering framing subchannel could be zeroed for transmission through the DCS. The downstream DNC hardware would then reinsert the framing subchannel.

Since the CRF interfaces with the TD-1192, if TRI-TAC or AII access at a station without TD-1192s or without enough TD-1192s to handle the TRI-TAC or AII traffic, then additional TD-1192s would have to be deployed along with the CRF. DNC hardware at the group level interfaces the TD-1193s and hence does not require the additional cost of deploying more TD-1192s. Also, at sites where both 64 kb/s and 16/32 kb/s channel reassignment is required, use of the CRF requires the deployment of the DNC "A" function shown in Figure 4-2, since the CRF cannot reassign 64 kb/s channels within T1 digital groups. The DNC "B" function hardware can reassign 64 kb/s channels; hence "A" function hardware is not required and could be eliminated if the size requirement for 64 kb/s reassignment at the station in question is small.

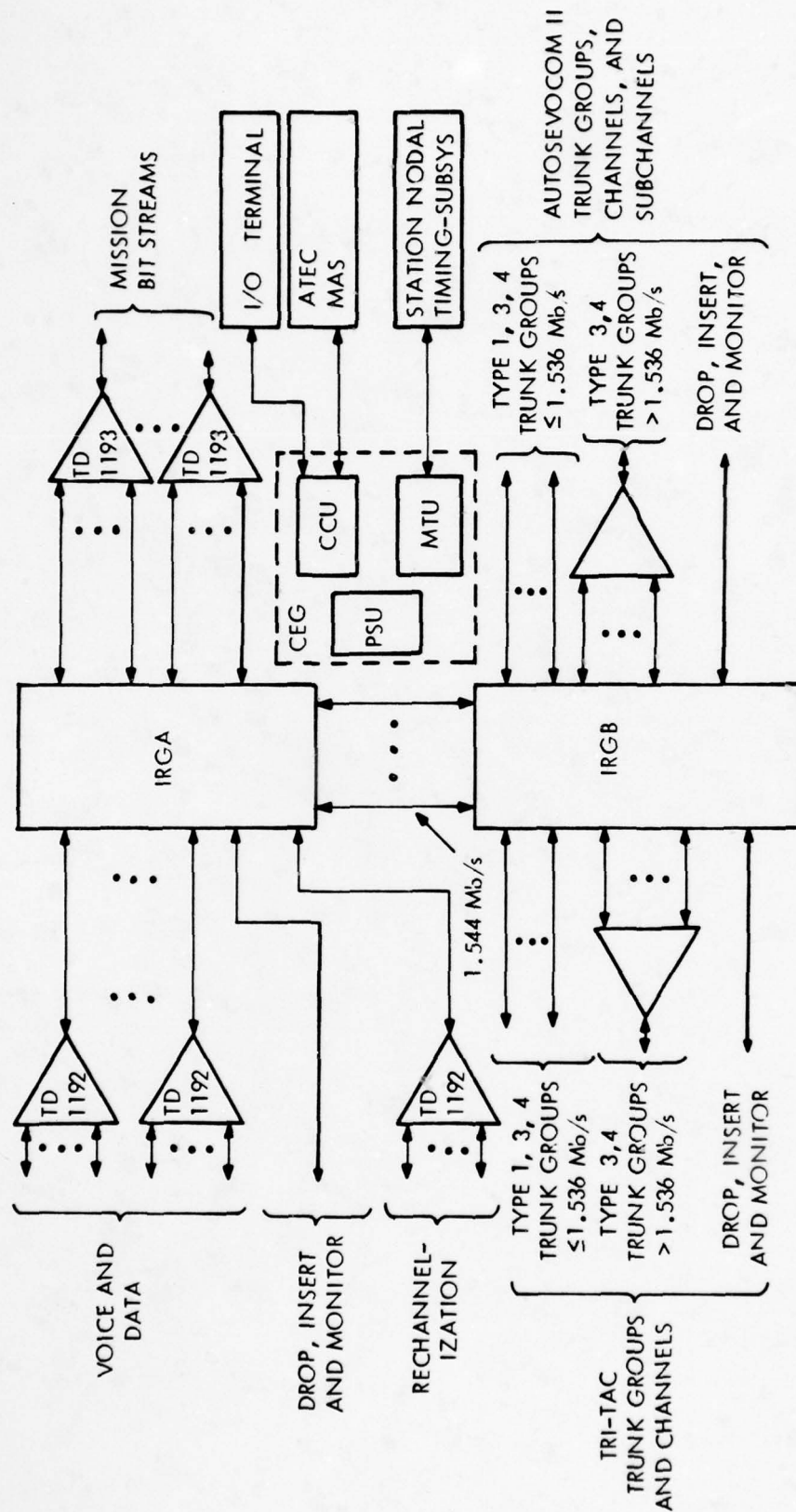
The conclusion is that deployment of the CRF at the channel level is not adequate to meet the requirements of the DNC "B" function. Since it is beyond the scope of this study to determine if the CRF could be modified to operate more effectively in a DNC role, it is recommended that this study proceed with the design of hardware to perform the DNC "B" function.

## 6.2 FUNCTIONAL DESCRIPTION

Digital Network Control can be functionally divided into two parts, channel reassignment and control. Channel reassignment is provided by the Digital Control Element (DCE) and is the function which makes automatic DNC possible. Control refers to the control and coordination of the DCEs in a network, and interfacing the DCEs with man.

### 6.2.1 Digital Control Element (DCE) Description

Figure 6-1 shows the DCE as it is deployed at a DCS station. It consists of three hardware groups, Interface and Reassignment Group A (IRGA), Interface and Reassignment Group B (IRGB), and the Common Equipment Group (CEG). The IRGA provides interfacing and reassignment of 64 kb/s PCM channels within T1 digroups while the IRGB handles 16 and 32 kb/s channels and 2 and 4 kb/s subchannels within TRI-TAC formatted digital groups. The CEG provides functions common to both the IRGA and IRGB such as power and timing.



## NOTE:

- IRGA - INTERFACE AND REASSIGNMENT GROUP A
- IRGB - INTERFACE AND REASSIGNMENT GROUP B
- CEG - COMMON EQUIPMENT GROUP
- CCU - CENTRAL CONTROL UNIT
- MTU - MASTER TIMING UNIT
- PSU - POWER SUPPLY UNIT

Figure 6-1. DCE - Station Configuration

The CEG is required for all DCEs, whereas the IRGA and IRGB are optional. A DCE may be configured to have only an IRGA, only an IRGB, or both. The interface between the IRGA and IRGB is the standard T1 format. This satisfies the DNC A and B functional modularity as required in Section 4.2, permitting the DCE to be tailored to provide only those functions required at each site where it is deployed.

#### 6.2.1.1 Interface and Reassignment Group A (IRGA)

As shown in Figure 6-1, the IRGA is placed in the DCS transmission hierarchy between the TD-1192 and TD-1193. TD-1192s required for rechannelization are connected to the IRGA as required. Note that the number of T1s from TD-1192s does not necessarily equal the number from TD-1193s because of the presence of through groups. The IRGB and test equipment also interface the IRGA as T1s.

Figure 6-2 shows the IRGA hardware configuration. Each full-duplex T1 from a TD-1192, TD-1193, IRGB, or piece of test equipment is plugged into a connector which is wired to the DCE. The receive side of each T1 is connected to the Input Framing Unit (IFU) and the transmit side is connected to the Output Framing Unit (OFU). In Figure 6-2, the ports numbered 1 on the IFU and OFU make up a termination on the IRGA for a full-duplex T1. The IFU and OFU provide the functions necessary for frame synchronization and alignment and are discussed in detail in Section 7.2.2.1.

The Data Memory Units (ADMU) and the Output Control Units (AOCU) provide the digital time division switching capability as discussed in Section 5. The "A" prefix indicates that these units are part of the IRGA. Data is written into the ADMUs and read out by the AOCUs, accomplishing the switching function. Analysis has determined that double buffered data memories and byte transfers (refer to Section 5.2.2.1) result in the greatest reduction in redundancy. Referring to Figure 6-2, data is written into all the ADMUs in a row (i.e., all ADMUs in a row always contain the same data bits), hence the number of ADMUs in a row indicates the redundancy. In the figure, the redundancy is four (the hot standby column is not counted).

Each AOCU can be read from any ADMU in its column; therefore, it has access to the data bits of all T1s. Each row handles the data from 32 T1s. After conversion to 8-bit parallel bytes, the 32 digroups are multiplexed together in the IFU and then written into a row of ADMUs. Similarly, each AOCU handles the output for 32 digroups. The OFU demultiplexes them and converts them back to serial. The figure shows nine parallel lines into a row from the IFU because a parity bit is added to the eight data bits.

The IRGA is modular in groups of 32 T1s. Ignoring the spare column for the moment, a minimum IRGA would have one ADMU (in the figure, the ADMU in the upper left) and one AOCU (the AOCU on the left). This configuration can handle up to 32 T1s which may be from first- or second-level multiplexers, the IRGB, test equipment, or any



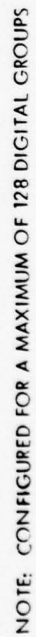


Figure 6-2. Interface and Reassignment Group A

combination. To expand, immediately beyond 32 digroups, the three ADMUs adjacent to the upper left-hand ADMU are added as well as another AOCU. Now the IRGA can handle up to 64 Tls. The IRGA can be configured in this manner for any multiple of 32 up to 192 by growing outward from the upper left corner. The largest IRGA (192 Tls) uses 36 ADMUs and 6 AOCUs (not counting spares). Figure 6-2 is shown for a maximum of 128 Tls. The IFU and OFU are also modular, the former in increments of five digroups and latter in increments of eight. This satisfies the modularity requirements discussed in Section 4.2.

The spare units are provided for automatic fault correction. Selectors in the OFU allow the spare column to substitute for any other IRGA column. Prior to substitution, the address memory in the spare AOCU is updated to match that of the AOCU in the column for which the spare column is to be substituted. The spare column is modular and always has one spare ADMU and the spare AOCU. Additional spare ADMUs are added as the number of rows increases. Further discussion of automatic fault correction can be found in Section 6.3.4.

#### 6.2.1.2 Interface and Reassignment Group B (IRGB)

The Interface and Reassignment Group B (IRGB) block diagram is shown in Figure 6-3. The operation is similar to that of the IRGA in that data is written into the rows of BDMUs, and read out of the columns by the BOCUs. The IRGB expands in a manner like that for the IRGA. Each BDMU and BOCU accepts a maximum of three digroups instead of 32, as with IRGA. Single buffered data memories and bit transfers are employed, unlike the IRGA, which uses double buffering and byte transfers. This is necessitated by the different format of the TRI-TAC formatted channels. PCM channels are byte-interleaved while TRI-TAC channels are bit-interleaved. Hence, it is a simple matter to convert a PCM channel to 8-bit parallel but impractical to convert the TRI-TAC channels to parallel. Figure 6-3 shows four lines into a row from the Input Framing and Conversion Unit (IFCU) because parity is added to the three digroups, as in the IRGA.

The IRGB differs in many other respects from the IRGA due to the different channel rates and digital group formats. The IFCU and the Output Framing and Conversion Unit (OFCU) must handle TRI-TAC formatted digital groups as well as Tls. These trunk groups may be either AUTOSEVOCOM II or tactical groups. The IFCU and OFCU perform frame synchronization and alignment for these groups. Since the BDMUs and BOCUs operate on Tl digroups, the TRI-TAC format trunk groups must be put into this form by the IFCU. It multiplexes groups together to form 1.536 Mb/s bit streams and stuffs this to 1.544 Mb/s, the digroup rate. The OFCU performs the reverse process. Note that Tls coming to the IRGB from the IRGA need not be synchronized because they have already been by the IRGA, but the TRI-TAC formatted groups within the Tls must be major-frame aligned to the other digital groups connected to the IRGB. The groups in the Tl are already minor-frame aligned with respect to the IRGB digital groups because the Tl is frame aligned to the internal IRGB digroups, as mentioned above, and because

SRS - SUBCHANNEL REASSIGNMENT  
SUB-GROUP

BDMU - DATA MEMORY UNIT

BOCU - OUTPUT CONTROL UNIT

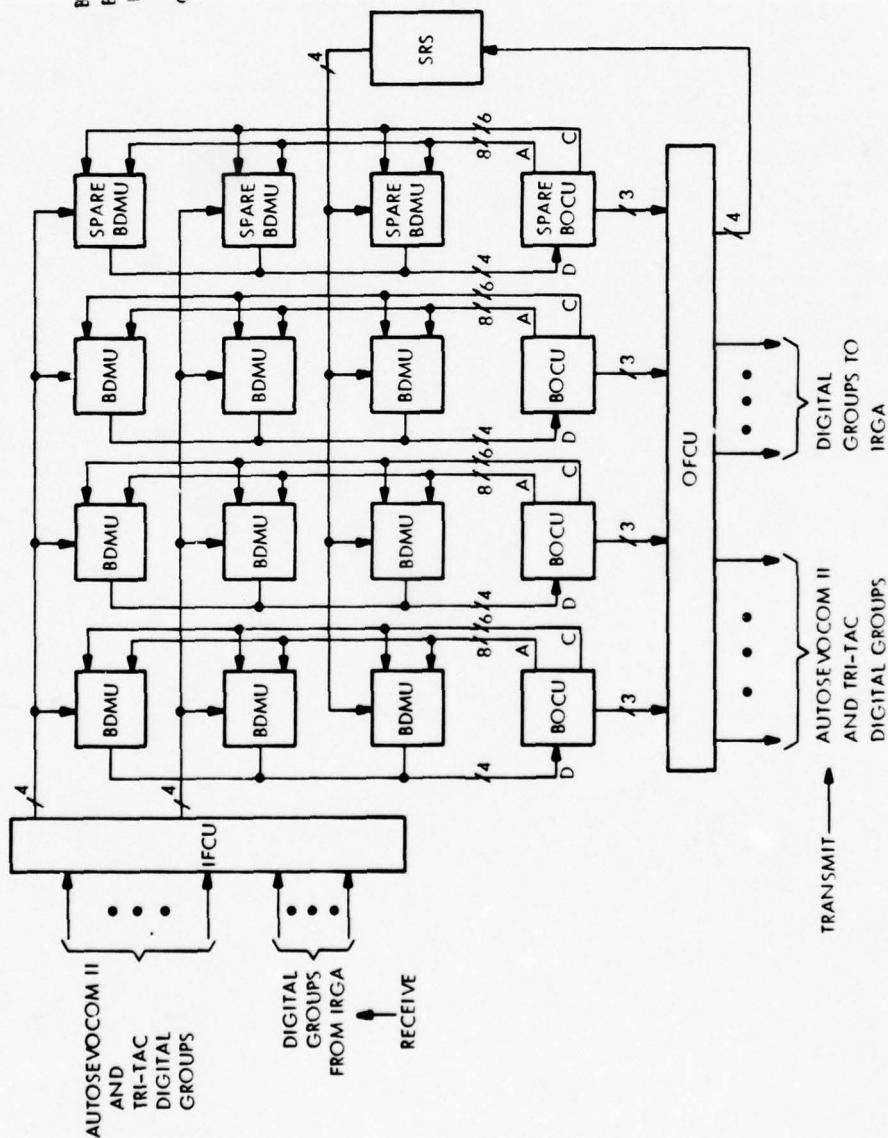
IFCU - INPUT FRAMING AND  
CONVERSION UNIT

OFCU - OUTPUT FRAMING AND  
CONVERSION UNIT

D - DATA BUS

A - ADDRESS BUS

C - CONTROL BUS



NOTE: CONFIGURED FOR A MAXIMUM OF 3- 1.536 Mb/s DIGITAL GROUPS

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Figure 6-3. Interface and Reassignment Group B



the T1 frame period is a multiple of the TRI-TAC format minor-frame period. If no IRGA is deployed, then the IRGB must synchronize and align any T1s connected to it.

The IRGB also contains a Subchannel Reassignment Subgroup (SRS) which handles reassignment of 2 and 4 kb/s subchannels. It accepts up to three internal T1 digroups from the BOCUs. The BOCUs extract overhead channels from the digital groups and insert them in the digroups to the SRS. The SRS stores an entire major-frame of overhead channels, giving it access to each subchannel. After reassignment of the subchannels, the overhead channels are sent to a row of BDMUs where the BOCUs can then insert the subchannel reassigned overhead channels back into their proper places. The SRS contains an SDMU and an SOCU which are very similar to the BDMU and BOCU in operation. Alternative approaches to subchannel reassignment involve special hardware to extract overhead channels from the trunk groups. This is a more complex and more expensive approach than using the BDMU/BOCU extraction method just described.

An important factor in the operation of the IRGB is the relationship between the T1 and TRI-TAC formatted frame periods. The T1 frame period is 125 msec while for 16 kb/s digitalization the TRI-TAC format minor frame period is 62.5 msec and for 32 kb/s digitalization the minor frame period is 31.25 msec. This means that the T1 frame period is an integral multiple of the TRI-TAC format minor frame which allows the T1s and digital groups to be aligned such that the start of a minor frame coincides with the start of a T1 frame. Also, each T1 frame with 16 and 32 kb/s channels imbedded in it will contain two bits from each 16 kb/s channel and four bits from each 32 kb/s channel.

#### 6.2.1.3 Common Equipment Group (CEG)

The CEG as shown in Figure 6-4 consists of the hardware common to both the IRGA and IRGB. The Central Control Unit (CCU) controls the hardware discussed above and interfaces it to the outside world. The CCU connects to the hardware via a bus system; to the ATEC Communications Interface Function (CIF) which provides a link to both the station controller's terminal and the Nodal Control Subsystem (NCS); and to a local terminal for backup purposes.

The Master Timing Unit (MTU) receives a master clock signal from the DCS station timing subsystem or derives it from the appropriate transmission link. Based on this master signal, the MTU generates all timing signals needed by the DCE. It also provides a free-running capability in the event of a failure in the master timing source. The Power Supply Unit (PSU) provides power to the IRGA, IRGB, CCU, and MTU.

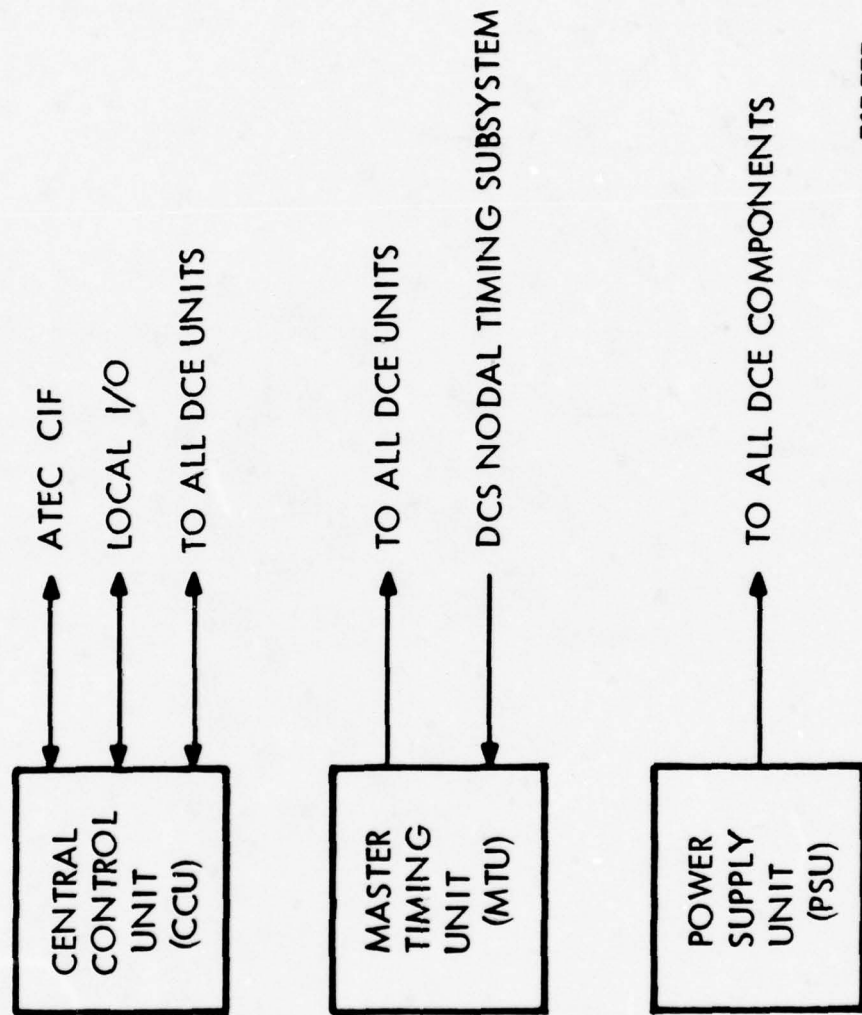


Figure 6-4. Common Equipment Group

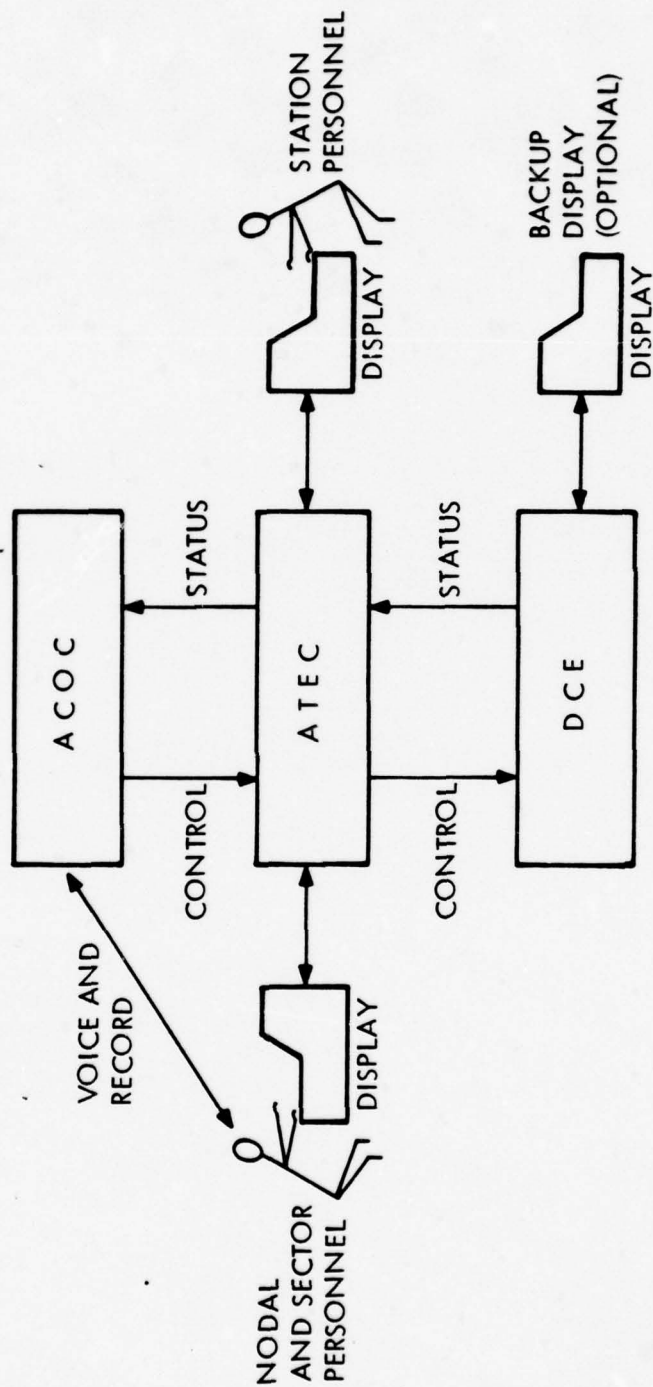
### 6.2.2 DCE Control

As the ratio of communications cost to processing costs increases, it becomes advantageous to place more control functions near the system or device to be controlled rather than centralizing all control functions. A properly designed decentralized control system has the added advantage of increased performance, availability, and survivability [Reference 6-1]. The planned DCS system control subsystem, which is discussed in Sections 2.3 and 3.1, will employ a hierarchical structure with decentralized control. Control of the DCEs is to be provided by a hierarchical structure which is physically integrated into the planned system control subsystem. This realizes the advantages described above and additional cost savings by permitting the sharing of facilities between DNC and system control.

The basic control hierarchy is shown in Figure 6-5. Control flows downward in the structure while status information flows upward. Station nodal and sector personnel access and control the DCE via ATEC (refer to Section 3.1 for a description of ATEC capabilities in this area). For example, both the DCE and the Station Controller Terminal Function are connected to the colocated Communication Interface Function at a station and would communicate through this device. Should ATEC fail to be deployed, DNC would utilize whatever manual or automated control and information distribution system is implemented at the three lower levels of the planned system control subsystem. The ACOC could access a DCE automatically through ATEC or, as is the recommended approach, indirectly by voice or record communication with sector personnel. A display may be plugged directly into the DCE for fallback purposes if trouble occurs within ATEC. The advantage of this DCE access and control scheme is that it uses the planned ATEC communications facilities instead of requiring a separate control system. The effect of this decision on the human interface is discussed further in Sections 6.3.1 and 6.3.2.

Functional control of the DCE hardware is distributed between the DCE CCU and software located at the node and sector levels. The software which interfaces the DCE with system control personnel is located in the Nodal Control Subsystem (NCS) and the Sector Control Subsystem (SCS) of ATEC because this places it closer to the point where most control decisions are made. This is beneficial since it permits easy access to the ATEC data base located in an NCS or SCS. The DCE control software will need the information in the data base so colocating the two eliminates the need for a duplicate data base for the DCE. Alternatively, this software could run on the CCU and access the nodal data base via the ATEC communications facilities, but this approach would result in a higher load placed on these facilities by the DCE than if this software were colocated with the data base. Also, the DNC software in the NCS and SCS can share some software with ATEC, such as data base and I/O routines.





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Figure 6-5. DCE Control Hierarchy

The CCU provides control of alterations to the address memories and of fault detection and isolation within the DCE. These functions are placed within the DCE because this puts the control near what it is controlling. A larger burden would be placed on the ATEC communications facilities if these functions were placed in the NCS. Some human interface functions are performed by the CCU in order to support the backup display.

### 6.3 OPERATIONAL ALGORITHMS

The operational algorithms of Digital Network Control can be classified into five categories: man/machine interface, functional algorithms, fault tolerance, initialization and recovery, and synchronization. These algorithms encompass both implementation aspects (e.g., synchronization procedures) and control aspects (e.g., DCE operational commands) of DNC. Each of the five categories is discussed below.

#### 6.3.1 Man/Machine Interface

The normal man/machine interface for DNC consists of an ATEC Controller Terminal Function (CTF) and the software to support it. According to human engineering principles, one common control console is preferable to two separate panels. With this commonality it is then important that the type of dialogue that personnel conduct with DNC software be the same as the type of dialogue used with ATEC. For example, if ATEC employs a prompt-oriented dialogue where the user fills in blanks and makes selections, then DNC must also use this type of dialogue. Similar types of dialogues for the various system control functions help to reduce training time and operator error.

A dialogue type is not specified in the ATEC System Description Requirements Document [Reference 6-2], so for this study a simple command/response system was assumed. System Control personnel enter a DNC command at a CTF and this command is sent to a SCS or NCS. There the DNC software analyzes the command and if the command is invalid in some respect, returns an error message. If the command is valid, the software accesses the data base and generates and transmits the appropriate machine-level commands to the DCEs. Upon completion of the operation, a message is returned to the controller who originated the command which indicates the successful execution of the command. If the command could not be executed, the reason for the failure is provided.

All commands will return some response within 10 seconds from the time the command is entered. Commands which take longer than 10 seconds to complete will return an acknowledgement to let the controller know that the command was accepted [Reference 6-2]. Again, this is only a preliminary dialogue structure chosen for its simplicity. If a different type is specified for ATEC, DNC will conform to that approach.

### 6.3.2 Functional Algorithms

This section discusses how the DCE is used to perform the functions of DNC presented in Sections 3 and 4. Scenarios are used to present some of the functions and indicate how personnel are involved.

The system must be designed to be flexible in order to accommodate new functions and control algorithms different from those described here. DNC functions are classified into two groups, static and dynamic. Static functions are long-term functions in which the related channel connectivity remains relatively fixed. Dynamic functions are those which are employed for more frequent connectivity changes.

#### 6.3.2.1 Static Functional Algorithms

Five of the requirements and benefits of DNC discussed in Sections 3 and 4 fall into the category of Static Functions. They are the elimination of backhauling, network flexibility (rechannelization), TRI-TAC interface, AUTOSEVOCOM II interface, and equipment savings. These are based on the DCE's ability to connect any channel to any other channel on a long-term basis while the dynamic functions are based on the ability to alter the channel connectivity.

When a DCE is installed at a site, a data base is generated for the SCS/NCS with jurisdiction over the site (refer to Section 7.3.1.2.5). This data base contains the channel connectivity which provides the static functions listed above. If changes are required, data base routines are used to update the data base. The address memories in the DCEs are then reloaded to reflect the changes. The LOAD command, described in Section 7.3.2.4.2.8, performs this reloading function.

#### 6.3.2.2 Dynamic Functional Algorithms

The four dynamic DNC functions are reconfiguration, reroute, on- and off-line test, and loopback. All result in a change in channel connectivity with reconfiguration being a more permanent alteration than the temporary patch performed by the other three dynamic functions.

6.3.2.2.1 Reconfiguration - This DNC function is used when a circuit within the DCS is reconfigured, such as when a user moves from one site to another. After the user's Telecommunications Service Order (TSO) is processed and the new route through the DCS for his circuit is determined, personnel at the ACOC communicate this decision to personnel at the sector level. Here, ASSIGN commands (refer to Section 7.3.1.3.3.5) are entered into the SCS which in turn generates hardware commands to the DCEs involved in the route change. The success or failure of the operation is communicated back up to the ACOC. An alternative would have ACOC personnel enter the ASSIGN commands into the SCS via the ACOC processor; however, a direct ACOC processor to SCS data link is not planned at this time.



6.3.2.2.2 Reroute - Rerouting for restoral purposes is accomplished in a manner similar to that for reconfiguration. After the route has been selected, REROUTE commands (refer to Section 7.3.1.3.1) are issued for the DCEs involved. An example of a reroute action involves the situation shown in Figure 6-6. A trunk from KLN to NBG traverses link M0293. Assume that this link fails and the decision is made to reroute the trunk via FKT based upon a canned reroute plan stored in ATEC. The plan consists of three REROUTE commands, one for each of the three sites involved (FEL, BTL and FKT). Execution of the REROUTE commands causes the trunk in question to be rerouted to link M0070 at FEL, from M0070 to link M0366 at FKT, and from M0366 to M0299 at BTL. Note that if a trunk existed from FEL to BTL via FKT and this trunk was used for the reroute, then there is no need to alter the connectivity at FKT and therefore, the reroute plan would not contain a REROUTE command for FKT.

The controller who initiated execution of the plan can modify it depending upon the current circumstances prior to initiating execution of the plan. If none of the plans are satisfactory, the controller can create new plans made up of REROUTE commands. Alternatively, REROUTE commands can be issued directly without first creating a canned reroute plan in the SCS or NCS.

When the link is returned to service, the reroute is terminated. This action causes REROUTE TERMINATE commands to be executed for each site involved. In the example, the connectivity for the trunk would be restored to what it was prior to the reroute. Any trunks which were preempted would be automatically reconnected in their original configuration. For directly issued REROUTE commands the controller must issue the corresponding REROUTE TERMINATE commands.

Which level in the system control hierarchy initiates the reroute depends upon the extent of the reroute. If the reroute is solely within a node or sector, then it can be handled by the appropriate NCS or SCS. If the reroute spans more than one sector, then either the ACOC must coordinate the activities or the sectors involved must coordinate.

6.3.2.2.3 On- and Off-Line Tests - These two functions are used in conjunction with ATEC performance assessment and fault isolation procedures. The TEST, LOOPBACK, and MONITOR commands provide system control personnel with the capability to connect test gear to circuits and to loopback circuits. For example, when connecting a new access circuit from a station to a user, it could be checked out from the user location by looping the circuit back at the station. These commands could be used by ATEC directly, but most likely the off-line commands (TEST and LOOPBACK) will require human approval because they interrupt service.

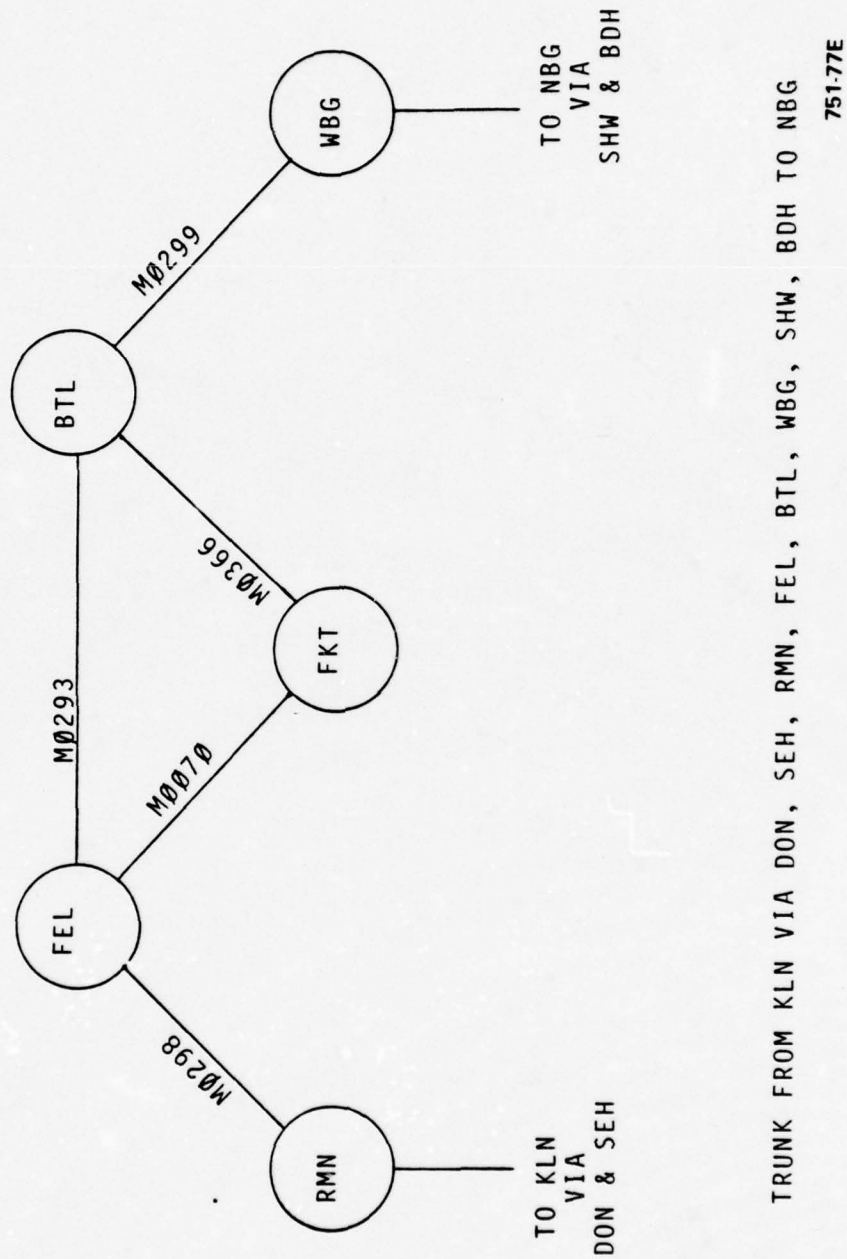


Figure 6-6. Reroute Scenario

The TEST command is used to check a circuit in an off-line mode. It provides the capability to connect a digital signal generator to the transmit side of a channel and a digital signal analyzer to the receive side of the channel. The LOOPBACK command provides for looping back a channel in either direction. These two commands, TEST and LOOPBACK, can be used jointly. For example, one end of a circuit is connected to test equipment and the other end is looped back. This test configuration can be implemented between any two stations in a circuit. The MONITOR command is an on-line command used to connect test equipment to a channel without interrupting service on that channel.

### 6.3.3 Fault Control

Fault control refers to the spectrum of actions taken to reduce the effects of faults and errors on system performance. There are several methods for dealing with faults: avoidance, detection, isolation, correction, and tolerance. Avoidance refers to design methodologies used to avoid design errors. Detection, isolation and correction deal with faults that actually occur and attempt to repair the failure. Tolerance refers to the system's ability to continue operation, possibly in a degraded mode, after a fault has occurred. Faults can occur both in hardware and software and both types are discussed below. The two are not independent in that hardware can check for software errors and vice versa.

#### 6.3.3.1 Hardware Failures

Hardware faults fall into three phases during the life of a device. The first phase consists mainly of manufacturing and design errors. After these are debugged, the second phase is entered which consists of Poisson distributed failures resulting from hardware deterioration. The final phase occurs near the end of the device's life when the incidence of failures increases. Fault control techniques for hardware are aimed at the second phase.

There are many techniques available for achieving a given level of hardware reliability and many are used in the DCE. Some, however, are too expensive for this application. Using high reliability components gets the problem at its source, while Triple Modular Redundancy (TMR) provides three copies of critical circuits and adds a voter circuit to output the majority result. Both techniques are better suited to systems which require very large MTBFs, such as spacecraft where manual repair is difficult or impossible. The DCE can be easily repaired by personnel and hence, the costs incurred by these two techniques are not warranted.

Three techniques are used in the DCE to detect hardware faults. In the first technique, parity bits are added to data words to check for problems in the data and address memories of the DMUs and OCUs, and to check the busses connecting them. Parity bits are



also added to information flowing between the CCU and other DCE units. Hardware parity checkers are employed in the DCE, with the exception that information going to the CCU is checked by software.

The second detection technique involves a comparison similar to the voting action of TMR. The output of an off-line unit is compared with that of an active unit. If the state and inputs are the same, then the outputs should also be the same. If the outputs fail to match, either the off-line or the active unit has failed. Comparing the off-line unit with a different active unit indicates which has failed. This technique is useful in a system where there are several copies of a particular circuit. Only one additional copy plus some comparison circuitry must be added.

The third technique involves software controlled testing of the hardware. The CCU will periodically test out its own components by running diagnostic software. The CCU will also check out the hardware fault control circuits, such as parity checkers and comparator, by inducing errors and watching for an error indication. For example, if a parity error is induced but no parity error was indicated, then the parity checker has failed.

For fault correction purposes, hot standby units are provided in a 1 for N redundancy configuration. This means that for every N circuits, which must be identical, one spare is provided which can be substituted for any one of the N circuits. Note that this spare can be used to perform the off-line comparison function described above. For a given number of circuits, N, the reliability can be increased by going to a 2 for N or greater degree of redundancy.

#### 6.3.3.2 Software Failures

Software failures differ from hardware failures in that only the first failure phase is present. Actually, only design errors are significant because manufacturing (i.e., duplication) errors are rare and easily detected. Hence, fault control techniques for software are aimed at detecting and isolating their impact on the system.

Each routine checks its inputs for validity. This is called the principle of mutual suspicion because each routine assumes that all others are faulty. This will detect many faults and prevent them from spreading further through the system. Inputs to a routine include arguments passed to it by the routine which called it, arguments returned to it by a routine which it calls, and information received from the outside world.

Another aid to software fault detection is to complete conditionals. This means that when a variable is tested for different values, all possible values are caught by some test. For example, if a variable can take on values from one to five and one of five

different actions is taken depending upon the value, an additional test is added to check for a value greater than five or less than one. The purpose is the same for validating inputs, but in this case, the variable being checked may be used solely within a routine.

To help prevent improper connections from being made due to software errors, a CCU lockout feature is provided. This is hardware implemented and, when activated, it blocks the flow of commands from the CCU to the other DCE elements. It is activated when a software error is detected or when a parity error is detected in a command from the CCU. It cannot be deactivated by the CCU, but requires human intervention to allow the CCU to continue control of the DCE.

#### 6.3.4 Initialization and Recovery

To initialize and bring up a DCE, the software at the NCS must first be installed and the data base generated (refer to Section 7.3.1.2.5). After power is applied to the DCE, the RESTART button is pressed which causes a RESTART interrupt (refer to Section 7.3.2.3.1). The CCU initializes itself and requests that the system tables be loaded. After they are loaded, the CCU is ready to accept a LOAD command to initialize the address memories which starts the flow of information through the DCE.

Recovery from a power failure does not involve human intervention. When power returns, the CCU automatically initializes itself and reloads the address memories. It then continues processing where it left off when the power failure occurred. Note that this requires a battery backup for the CCU RAM. If this is not provided, then a manual RESTART must be performed. Recovery from a CCU hardware or software failure requires a RESTART operation. The address memories should be reloaded in case the connections were made improperly by the CCU prior to detection of the error and the subsequent activation of the CCU lockout.

In the event that the CCU is isolated from the NCS (e.g., the station telemetry system fails), the DCE will operate in a fall-back mode. The station controller, via the Controller Terminal Function, or local backup terminal, can still command the DCE to alter the channel connectivity, but now he must use connection addresses instead of the normal format (e.g., TFELM029801112, which indicates direction, site, link, supergroup, group, and channel). He can perform the translation by calling a node on an orderwire and having personnel at the node access the data base and return the result to him. Alternatively, each site could have a listing of the connection address/channel mapping, which is periodically updated. All connectivity changes made during this fall-back condition are saved by the CCU on a list. When communications between the NCS and DCE are restored, the NCS uses this list to update its data base.

## 6.4 SYNCHRONIZATION

A description is provided of the methods and algorithms that the DCE employs in order to synchronize the channel reassignment function so as to maintain BCI in all channels. Master frame synchronization is discussed only with respect to DRAMA equipment. The algorithm used to synchronize the digital groups received from AUTOSEVOCOM II and TRI-TAC is the same as that specified in Reference 6-3 and therefore, will not be discussed. DNC timing results are based on the availability of an accurate and stable DCS timing reference as described in Section 4.4.2.

### 6.4.1 Master Frame Synchronization

This section describes the algorithm used by the Input Framing Unit (IFU) to establish and maintain master frame synchronization in each T1 digital group received from a TD-1192, TD-1193, or another DCE. The T1 frame structure is D2/D3 compatible and is shown in Figure 4-5. The algorithm is designed for a random error environment of no more than 1 error per 1000 bits [Reference 6-4].

The algorithm operates in two modes, frame maintenance and frame acquisition. In the frame maintenance mode, the IFU assumes that it is in-synchronization and monitors the receive direction for loss of synchronization. In the acquisition mode, the IFU assumes that it is out-of-synchronization and monitors the receive direction for the correct synchronization position. If the IFU is in the maintenance mode and determines that it has lost synchronization in a particular digital group, it switches to the acquisition mode for that group. The IFU returns to the maintenance mode only after it determines that it has relocated the correct synchronization position.

In each mode of operation, a 16-bit sync word is formed using 16 consecutive bits from the assumed synchronization position. If the IFU is in synchronization and neglecting the occurrence of bit errors, the correct sync word consists of either the 1010...10 pattern or the 0101...01 pattern. If the IFU is out-of-synchronization, the sync word consists of a random string of 16 bits. Each time a complete sync word is formed, it is correlated against one or both correct sync word patterns, depending upon the IFU mode. If the IFU is in acquisition mode, both correlations are performed and the following rules apply:

- a. If either correlation results in no disagreements, declare an in-sync condition, flag the framing bit position and the correct sync pattern, switch to the maintenance mode, and check the next sync word for frame maintenance.
- b. If both correlations result in at least one disagreement, remain in the acquisition mode, displace the synchronization position one bit, and check the next sync word for frame acquisition.



If the IFU is in the maintenance mode, the correlation is performed against the last correct sync pattern and the following rules apply:

- a. If the correlation results in three or fewer disagreements, remain in the maintenance mode and check the next sync word for frame maintenance.
- b. If the correlation results in four or more disagreements, declare an out-of-sync condition, switch to the acquisition mode, displace the synchronization position one bit, and check the next sync word for frame acquisition. When switching from maintenance to acquisition, the acquisition mode first checks  $\pm 2$  bits from the last correct synchronization position per Reference 6-3 specifications.

The algorithm just described results in the synchronization performance shown in Table 6-1. Comparison of this table with Table 4-2 reveals that the DCE meets or exceeds all frame synchronization requirements.

TABLE 6-1. DCE T1 FRAME SYNCHRONIZATION PERFORMANCE

A.	FRAME ACQUISITION	PERFORMANCE
I. Start-Up		
	1. Time to Acquire Sync	<50 msec
	2. Probability of Acquiring	.98
	3. Probability of False Acquisition	.02
II. Following Loss of BCI ( $\leq \pm 2$ Bits)		
	1. Time to Detect and Reacquire Sync	<8 msec
	2. Probability of Acquiring Sync	.98
B. FRAME MAINTENANCE		
	1. Mean Time to False Loss-of-Sync	39 Hours

#### 6.4.2 DCE Timing

The DCE will provide group buffers within the IFU for each terminating digital group. These buffers compensate for transmission delay variations and timing differences between the DCE master timing unit and the recovered clock for each digital group.

Estimates of the effects of transmission delay variations are discussed below:

a. Coaxial Cable

1. The dominant cause of delay variations is linear expansion caused by temperature change.
2. Changes in transmission delay occur slowly.
3. For a path length of 3000 miles and a transmission rate of 1.544 Mb/s, the change in the number of bits stored in a cable due to a 22°C temperature change is approximately 10 bits.

b. Microwave Radio

1. Delay variations are caused by changes in temperature, pressure humidity, and rain.
2. Rapid and long-term delay variations are possible.
3. Average variations in link bit storage are daily, 0.5 bits; monthly, 2.5 bits; and yearly, 7.5 bits.

c. Troposcatter Transmission

1. Short-term variations are to be expected; however, the magnitude of these variations are not significantly greater than those experienced in LOS radio links.

d. Satellite Transmission

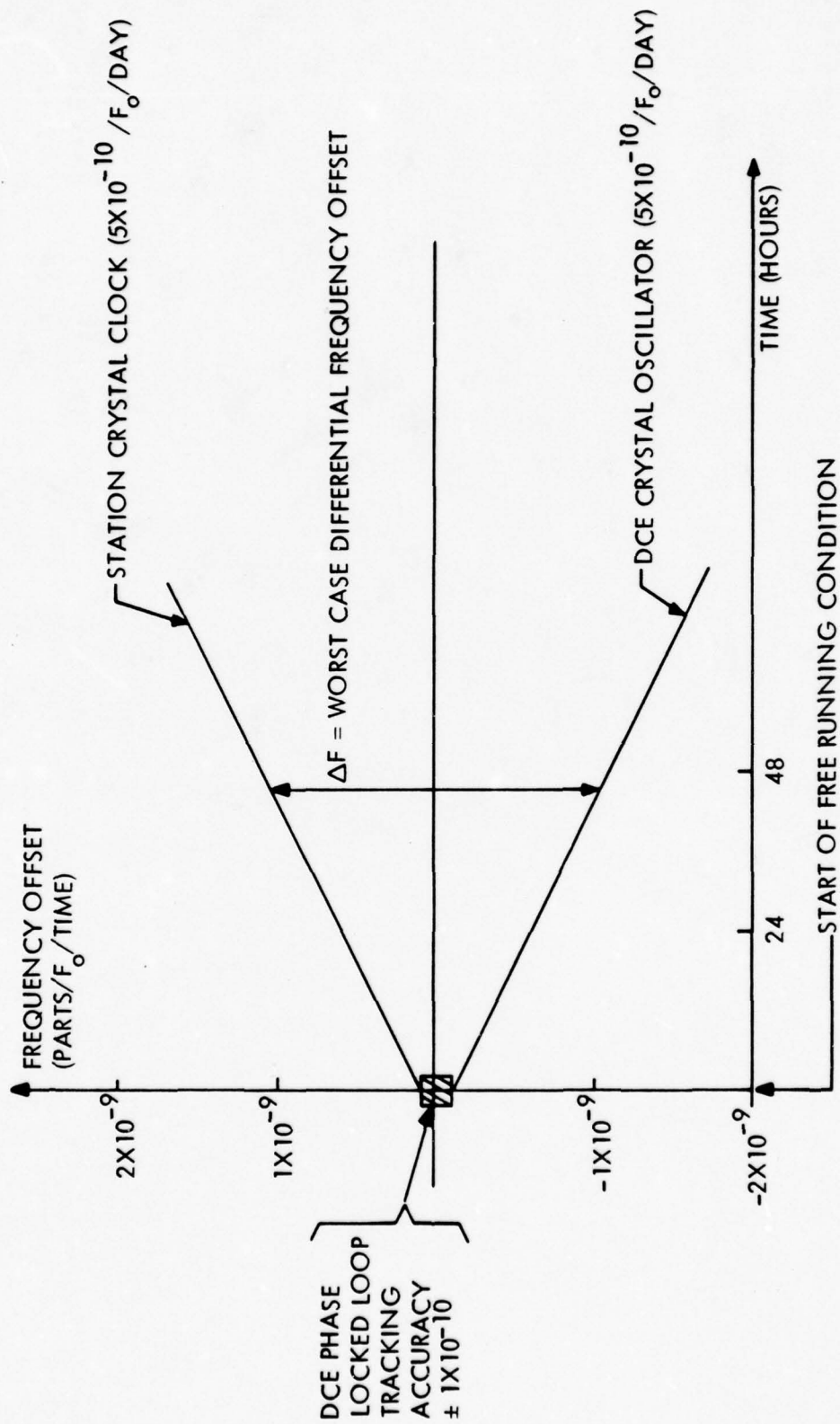
1. Delay variations in a satellite link during a 12-hour period can be quite severe, due primarily to orbital eccentricity. Buffer requirements for such links on the order of 5000 to 6000 bits are possible. However, this buffering is provided by the satellite ground station and need not be considered a DCE requirement.

Based on the above estimates of delay variations, 20 bits of capacity will be allocated to transmission delay variations in each digital group buffer.

The buffer capacity required to compensate for timing differences is determined for the situation in which the DCE is isolated from the station timing supply and the station timing supply is isolated from its DCS master. It is assumed that both timing supplies employ crystal oscillators instead of atomic clocks. Designing to this worst-case situation ensures that sufficient buffer size is allocated. The required buffer to provide a 24-hour free run capability for the DCE is 186 bits. The details of the calculations are shown in Figure 6-7. The clock stabilities shown in this figure are conservative values based on commercially available crystal clocks.

It follows from the results of this section that the total capacity of each digital group buffer must be at least 206 bits, 20 bits for transmission delay variation compensation and 186 bits for clock difference compensation.





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$\text{BUFFER REQUIREMENT FOR 24 HOURS} = 2 \times \int_0^{86400} \Delta F dt = 186 \text{ BITS}$   
 NOTE: TRANSMISSION RATE = 1.544 MB/S

Figure 6-7. Master Timing Unit Buffer Requirement

## SECTION 7

### DCE IMPLEMENTATION

This section provides the hardware and software details of a conceptual DCE implementation. Section 7.1 discusses the hardware/software trade-offs involved in the DCE implementation. Section 7.2 provides the hardware description of the DCE, and Section 7.3 provides the DCE software description. Finally, the DCE R/M/A considerations are discussed in Section 7.4.

#### 7.1 HARDWARE/SOFTWARE TRADE-OFFS

Several guiding principles were followed in the partitioning of the DCE functions into hardware and software. These principles and examples of their application to the DCE implementation are presented in the following sections.

##### 7.1.1 Use of Support Hardware to Reduce Software Complexity

Support hardware (such as microprocessor programmable peripheral interface and communications chips) reduces software complexity and hence development cost. This is especially important in lower production volume systems like the DCE.

This principle was applied to the design of the Central Control Unit (CCU) which is a microcomputer based on the 8080A microprocessor. This design utilizes the following 8080A support chips to substantially reduce the 8080A software size and development cost:

- a. 8251 Programmable Communication Interface Chip - This chip is used to provide the CCU interface with System Control and with a local TTY. The 8251 relieves the 8080A of a considerable amount of communications related processing with a considerable savings in 8080A software.
- b. 8255 Programmable Peripheral Interface Chip - This chip is used to provide the CCU interfaces with IRGA and IRGB.
- c. 8214 Priority Interrupt Control Unit Chip - This chip relieves the 8080A of some of the interrupt responsibilities with a corresponding decrease in the amount of interrupt software required.

### 7.1.2 CCU Fail Soft Operation

A failure of the CCU will not affect the operation of the DCE. Specifically, the DCE digital group interfaces and the flow of bits through the DCE switching matrices are unaffected by CCU failures. This requires that certain critical functions such as frame synchronization not be resident in the CCU. The DCE design discussed utilizes satellite microcontrollers to handle the synchronization functions. These satellite synchronization units operate completely independent of the CCU.

### 7.1.3 Flexibility Requirements

Human interfaces and data processing are two DCE functions requiring flexibility and hence were implemented in software.

### 7.1.4 Implement High-Speed, Real-Time Functions with Hardware

The DCE switching matrix read/write control is implemented in hardware because of the high-speed requirements of this function. Also, a CCU failure will not affect the operation of this important DCE function.

### 7.1.5 Utilize Microprocessors to Replace Random Logic

In many cases, it is cost-effective to replace random logic hardware implementations with microprocessors and their attendant firmware.

This approach was utilized in the frame synchronization function. A random logic implementation of the frame synchronization function for one input digital group requires approximately 1-1/2 6-inch by 10-inch printed circuit cards of random logic. The selected 2900 bit-slice microprocessor approach requires one printed circuit card for 5 input digital groups. Thus, the use of a microprocessor to implement the frame synchronization function results in a 7.5:1 reduction in printed circuit cards over the random logic approach.



## 7.2 HARDWARE ARCHITECTURE

The DCE hardware is partitioned into three groups:

- a. Interface and Reassignment Group A (IRGA)
- b. Interface and Reassignment Group B (IRGB)
- c. Common Equipment Group (CEG).

A hardware family tree of the proposed DCE implementation is shown in Figure 7-1. The relationship of these groups to one another is shown in Figure 7-1A which illustrates the DCE - Station Configuration.

The DCE can operate in the following configurations:

- a. IRGA, IRGB, CEG
- b. IRGA, CEG
- c. IRGB, CEG.

The following subsections present the details of the three DCE groups, the considerations involved in selection of components to implement these groups, and the physical packaging of the DCE.

### 7.2.1 Hardware Selection

This section presents the considerations involved in selecting an IC logic family for implementing the DCE groups. Also presented is the selection of a microprocessor family of ICs for implementing a frame synchronization microcontroller in the IRGA and IRBG.

#### 7.2.1.1 Selection of IC Logic Family

The most important consideration in selecting an IC logic family is the required component speed. This speed is characterized by the clock rate of the various registers and counters used to implement the DCE groups. Table 7-1 lists the four basic groups of clock rates and the candidate IC families compatible with these rates.

In the sections which discuss the hardware specifications of the two DCE reassignment groups (7.2.2.1 IRGA and 7.2.2.2 IRGB), it is shown that data flows through these groups at a 6.176 MHz rate. Because of considerations such as cumulative logic gate delays and multiple operations required during a 6.176 MHz clock period (162 ns), the actual DCE logic speed requirement is in excess of 15 MHz. Thus the DCE can be classified as a medium speed system. Referring to Table 7-1, the DCE logic speed requirements can be met by use of either the LS-TTL and TTL logic families. CMOS logic is too slow for implementing the DCE circuits; S-TTL and ECL require high power and provide unnecessarily high speed; H-TTL is obsolete since it consumes more power than S-TTL, has similar interconnection problems, and offers only half the speed.

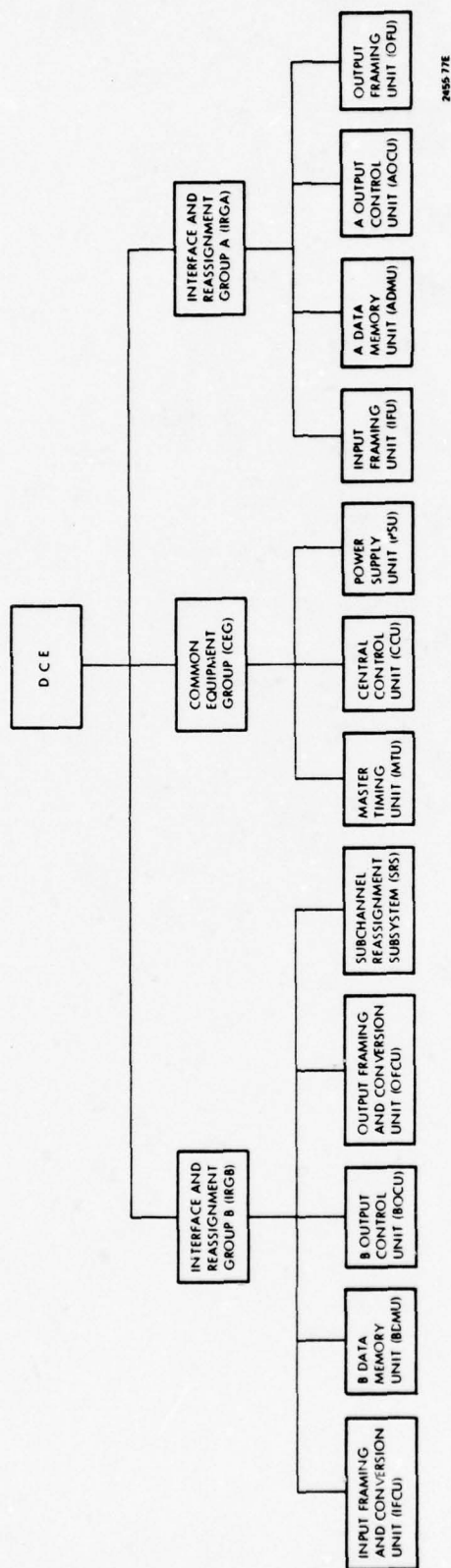
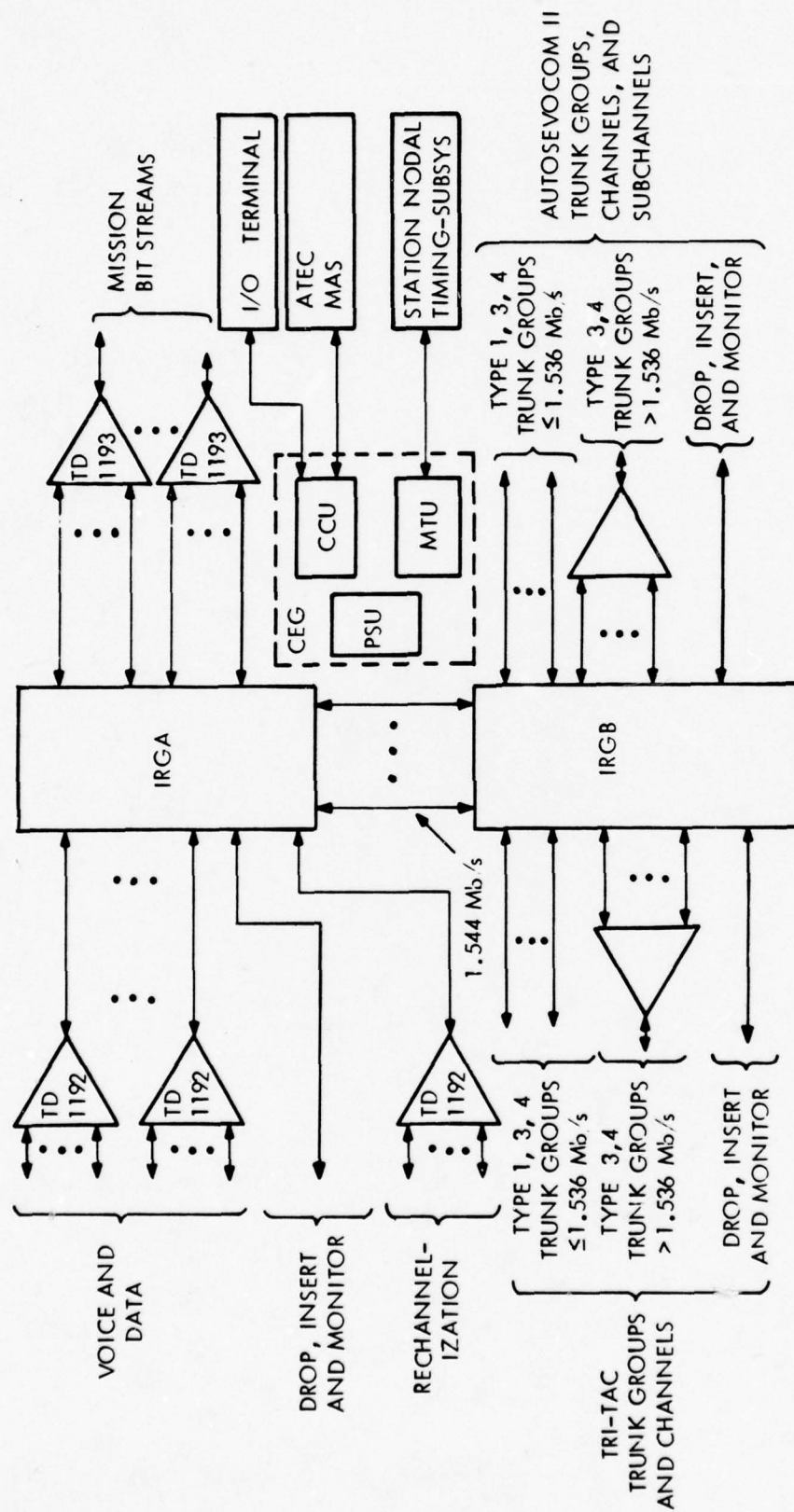


Figure 7-1. Hardware Family Tree of the Proposed DCE Implementation



**NOTE:**

IRGA - INTERFACE AND REASSIGNMENT GROUP A

IRGB - INTERFACE AND REASSIGNMENT GROUP B

**CEG - COMMON EQUIPMENT GROUP**

CCU - CENTRAL CONTROL UNIT

CCU - CENTRAL CONTROL UNIT  
MTU - MASTER TIMING UNIT

PSU - POWER SUPPLY UNIT

Figure 7-1A. DCE - Station Configuration

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TABLE 7-1. CANDIDATE IC FAMILIES VERSUS SYSTEM CLOCK RATES

CLOCK RATE	CANDIDATE IC LOGIC FAMILIES
Very High Speed (>100 MHz)	ECL
High Speed (30 to 100 MHz)	ECL, S-TTL, H-TTL
Medium Speed (5 to 30 MHz)	LS-TTL, TTL
Low Speed (<5 MHz)	LS-TTL, TTL, CMOS

NOTES: ECL = Emitter Coupled Logic  
TTL = Transistor - Transistor Logic  
S-TTL = Schottky TTL  
LS-TTL = Low Power Schottky TTL  
H-TTL = High Speed TTL  
CMOS = Complementary Metal Oxide Silicon

The two candidate IC families, TTL and LS-TTL, are compared in detail in the following paragraphs to determine the optimum choice for the DCE groups. The following criteria were used for making the final selection between TTL and LS-TTL.

- a. Technical parameters of the IC logic family
- b. Availability - number and variety of the ICs in the logic family
- c. Cost
- d. Reliability predictions
- e. Second-source availability.

7.2.1.1.1 Comparison of TTL and LS-TTL Technical Parameters - LS-TTL provides many advantages over standard TTL in the area of technical parameters. The following list is a summary of the advantages of LS-TTL over TTL:

- a. LS-TTL provides a reduction by a factor of 5 in the supply current and power over standard TTL. Less supply current allows smaller, less expensive power supplies, which reduces overall DCE cost, size and weight. Lower power consumption means less heat is generated, which simplifies thermal design. Packing density can be increased or cooling requirements reduced, or perhaps both.

The power reduction provided by the Low-Power Schottky technology provides an additional advantage. Standard TTL technology has now reached the level where the maximum IC complexity is often limited by IC package power capabilities. When IC designs are implemented with Low-Power Schottky TTL, IC complexities can increase by a factor of five greater than standard TTL designs without exceeding IC package power limitations. These more complex functions can reduce the number of packages required to implement the DCE and hence reduce cost.

Less noise is generated by LS-TTL, since the improved transistors and lower operating currents lead to much smaller current spikes than standard TTL, which means that fewer or smaller power supply decoupling capacitors are needed. In addition, load currents are only 20 percent of standard TTL which means that when a logic transition occurs, the current changes on signal lines are proportionately smaller, as are the changes in ground currents.

- b. LS-TTL is compatible with CMOS and MOS. Standard TTL is not fully compatible with most CMOS and MOS. The simplified MOS to TTL interfacing provided by LS-TTL results from the fact that the input load current of LS-TTL is only 25 percent of a standard TTL load. Most CMOS devices are designed to drive one LS-TTL input load at 5.0V. The LS-TTL can also interface directly with CMOS operating up to 15V due to the high voltage Schottky input diodes. LS-TTL is the best TTL to MOS or CMOS driver. With the modest input current of MOS or CMOS as a load, any LS-TTL device output will rise up to within 1V of  $V_{CC}$  (+5V), and can be pulled up to 10V with an external resistor.
- c. LS-TTL interfaces directly with other TTL families:
  - 1. Fan-out of (5) 7400 inputs or (4) 74S/74H loads
  - 2. Low input current provides increased fan-out for standard TTL source devices (LS-TTL) as a load)
- d. LS-TTL functions and pinouts are the same as the standard TTL devices. LS-TTL is also speed compatible with standard TTL.
- e. LS-TTL provides additional speed over standard TTL. LS-TTL gate delay is approximately one-half the gate delay of standard TTL. This means that in certain DCE applications, where the speed of standard TTL would be too slow, LS-TTL speed will be sufficient. This eliminates the need for special TTL families such as S-TTL.

7.2.1.1.2 Comparison of TTL and LS-TTL Availability - Number and Variety of ICs in The Logic Family - There are a large number of SSI and MSI functions available in standard TTL. Somewhat fewer device types are available in LS-TTL, but this is rapidly changing. In addition, LS-TTL has more complex functions due to the thermal considerations discussed in Section 7.2.1.1.1.

Table 7-2 illustrates a number of standard TTL and LS-TTL devices under broad function categories.

In those cases where an LS-TTL device is not available, the standard TTL can be used. The design can be upgraded to LS-TTL when the function becomes available.

TABLE 7-2. NUMBER OF DEVICES AVAILABLE

FUNCTION	STANDARD TTL	LS-TTL
Arithmetic Elements	6	4
Counters	15	13
Data Selectors/Multiplexers	7	8
Decoders	11	5
Encoders	2	0
Expanders	1	0
Flip-Flops	7	10
Gates	35	31
Latches	9	3
Registers	15	8
Schmitt Trigger	4	3
	<u>112</u>	<u>85</u>

NOTE: Source - Signetics Data Manual, 1976.

7.2.1.1.3 Comparison of TTL and LS-TTL Cost - Standard TTL and LS-TTL cost approximately the same. Table 7-3 provides a comparison of prices of ICs which are used to implement the various DCE groups. The prices of TTL and LS-TTL are very close. Summarizing Table 7-3 of 14 devices listed, 8 LS-TTL devices are priced lower than standard TTL and 6 LS-TTL devices are priced higher.

However, on a system basis, the use of LS-TTL devices will provide substantial savings over standard TTL. These savings will be in the areas of:

- a. More densely populated circuit boards resulting in fewer boards per system. This results from the lower dissipation of the LS devices.
- b. Substantially reduced power supply cost and reduced cooling costs.



TABLE 7-3. COMPARISON OF STANDARD TTL AND LS-TTL PRICES

IC TYPE NUMBER ①	DESCRIPTION	PRICES ②	
		STD-TTL	LS-TTL
7400/74LS00	Quad 2-Input Nand Gate	0.35	0.27
7404/74LS04	Hex Inverter	0.43	0.30
7408/74LS08	Quad 2-Input And Gate	0.37	0.27
7410/74LS10	Triple 3-Input Nand Gate	0.35	0.27
7432/74LS32	Quad 2-Input Or Gate	0.49	0.28
7437/74LS37	Quad 2-Input Nand Buffer	0.70	0.33
7474/74LS74	Dual D-Type Positive Edge-Trig. Flip-Flop	0.54	0.43
7493/74LS93	8-Line To 1-Line Data Sel./Mux.	0.55	0.95
74151/74LS151	8-Line To 1-Line Data Sel./Mux.	0.99	1.14
74153/74LS153	Dual 4-Line To 1-Line Mux.	0.99	1.39
74157/74LS157	Quad 2-Line To 1-Line Data Sel./Mux.	0.80	1.19
74174/74LS174	Hex D-Type Flip-Flop With Clear	1.42	1.28
74175/74LS175	4-Bit Binary Counter	1.21	1.28
74191/74LS191	Synchronous Binary Up/Down Counter	1.56	2.13

NOTES: ① Plastic Dual In-Line Package;  
Commercial/Industrial Temperature Range: 0°C to 70°C.

② Price based on quantity of 100-999.  
Prices from Fairchild DEM Price List - February 1977.

In summary, LS-TTL and standard TTL costs are approximately equivalent but LS-TTL usage will provide substantial overall system cost savings.

7.2.1.1.4 Comparison of TTL and LS-TTL Reliability Predictions -  
LS-TTL provides enhanced reliability over standard TTL. The reduction in supply current provided by LS-TTL means lower power dissipation on the chip. This causes less chip temperature rise above ambient, and lower junction temperature of the chip devices increases MTBF. Also, lower chip current densities minimizes metalization related failure mechanisms.

For example, if we compare the reliability of a typical MSI function in a system with an operating temperature of 55°C, a four times improvement in component failure rate can result from the lower junction temperature of a LS-TTL function versus a standard TTL function.

7.2.1.1.5 Comparison of TTL and LS-TTL Second - Source Availability -  
Both LS-TTL and standard TTL are widely available from several different vendors. Among those vendors supplying these two logic families are:

- a. Fairchild Semiconductor
- b. Motorola
- c. Texas Instruments
- d. Advanced Micro Devices
- e. Signetics
- f. National Semiconductor
- g. ITT Semiconductors
- h. Raytheon Semiconductor.

7.2.1.1.6 Selection of LS-TTL Logic Family - Based on the considerations outlined above, LS-TTL was chosen as the logic family for implementing the DCE.

The technical parameters of LS-TTL provide many advantages over standard TTL. The availability of both families is more than adequate to implement the DCE efficiently. The cost of both families is approximately the same, but LS-TTL provides many system cost benefits versus using TTL. In the area of component reliability, LS-TTL is superior to standard TTL. Finally, both logic families are widely multiple-sourced by all the major semiconductor manufacturers.

#### 7.2.1.2 Selection of Microprocessor Component Families

A microprocessor component family is required for implementation of the Framing Unit Microcontrollers in the IRGA Input Framing Unit and in the IRGB Input Framing and Conversion Unit.

7.2.1.2.1 Selection of Microprocessor Component Family for Implementing the IRGA and IRGB Framing Units - The Framing Unit provides frame acquisition, frame maintenance, and frame control for DCE input digital groups. If the Framing Unit were to be implemented using Medium Scale Integration (MSI) and Small Scale Integration (SSI) low-power Schottky TTL ICs, the resulting hardware would occupy approximately two printed circuit cards each containing about 60 16-pin DIPs. These 2 cards would perform the framing functions for only one digital group input.

An alternative approach utilizes a microprocessor based Framing Unit to provide the framing functions for five digital group inputs on a time-sharing basis. This approach which has been selected for the DCE requires only a single printed circuit card for five digital group inputs. The microprocessor is a Large Scale Integration (LSI) device which allows the large reduction in IC DIPs. The number of cards required is reduced by a factor of 10.

The instruction speed requirement on the microprocessor determines the technology which must be used. Analysis indicates that the speed requirements are such that there are no available MOS or CMOS microprocessors fast enough to meet the requirements. The speed requirement dictates that a bipolar bit-slice microprocessor component family must be selected. These units utilize bipolar circuitry. Table 7-4 lists various candidate bit-slice microprocessors considered for implementing the Framing Unit Microcontrollers.

TABLE 7-4. CANDIDATE BIPOLAR BIT-SLICE MICROPROCESSOR FAMILIES CONSIDERED FOR IMPLEMENTING THE IFU AND IFCU FRAMING UNIT MICROCONTROLLERS

PRIMARY VENDOR	BIT-SLICE MICROPROCESSOR FAMILY	BIPOLAR TECHNOLOGY USED
Fairchild	MACROLOGIC (9400)	Schottky TTL, I <sup>3</sup> L ①
Intel	3000	Schottky TTL
Motorola	10800	Emitter Coupled Logic
Texas Instruments	SBP0400A	I <sup>2</sup> L ②
Texas Instruments	74S481	Schottky TTL
Advanced Micro Devices	2900	Low-Power Schottky TTL
Monolithic Memories	6701	Schottky TTL

NOTES: ① Isoplanar Integrated Injection Logic  
 ② Integrated Injection Logic



These candidate bipolar bit-slice microprocessor families are now compared in detail to determine the optimum choice for the Framing Unit Microcontrollers. The following criteria were used for making the final selection:

- a. Second-source availability
- b. Number of different chips required
- c. Cost
- d. Software development support
- e. Technical parameters of the microprocessor family
- f. Number of bits per slice.

Table 7-5 provides the second-source availability details for each candidate family. Based on this information, the Motorola, Texas Instruments and Monolithic Memories families were dropped from further consideration. The multiple-sourcing of the 2900 family illustrates its popularity and the large segment of the bit-slice market it has captured. The remaining families are now compared with each other with respect to criteria b. through f.

TABLE 7-5. SECOND-SOURCE AVAILABILITY OF CANDIDATE BIPOLAR BIT-SLICE MICROPROCESSOR FAMILIES

PRIMARY VENDOR	BIT-SLICE MICROPROCESSOR FAMILY	SECOND-SOURCE VENDORS
Fairchild	MACROLOGIC (9400)	Signetics
Intel	3000	Signetics
Motorola	10800	None
Texas Instruments	SBP0400A	None
Texas Instruments	74S481	None
Advanced Micro Devices	2900	Motorola, Raytheon, Signetics, Sescosem National
Monolithic Memories	6701	None

7.2.1.2.1.1 Number of Bits Per Slice - The Intel 3000 family is a 2-bit wide slice family of chips. The AMD 2900 and Fairchild 9400 families are of the 4-bit wide slice variety. In general, the Intel 3000 series will require more IC packages to implement an 8-bit microprocessor for the Framing Unit.

7.2.1.2.1.2 Number of Different Chips Required - Table 7-6 indicates the types of chips and quantities required to implement an 8-bit Framing Unit Microcontroller based on each bit-slice component family. The table indicates that the 2900 family implementation utilizes the minimum number of IC packages, with the 3000 family a close second and the 9400 family a distant third. This is due to the fact that the 2900 and 3000 families use a higher level of LSI than does the 9400 family.

On the basis of this comparison, the 9400 family is eliminated from further consideration due to the high chip count it requires.

7.2.1.2.1.3 Technical Parameters of the Microprocessor Families - The 3000 bit-slice microprocessor family has seen very limited usage by the electronics industry compared with the 2900 family which is the largest selling bit-slice family. A few of the reasons for this are:

- a. The 3002 Central Processing Element utilizes a 28-pin package compared with the 2901 4-Bit Slice Microprocessor which utilizes a 40-pin package. The 28-pin package limits the number of inputs and outputs available and severely reduces design flexibility while increasing design complexity and hence development time. In addition, the pin limitation could increase requirements for extra firmware (PROM).
- b. The 3001 Microprogram Control Unit places limitations on memory jump instructions. The areas of program memory one can jump to is dependent on where in memory the jump will be from. This is a severe limitation and would probably lead to increased firmware requirements (additional software instructions in PROM).
- c. The 3000 instruction set is more complex than the 2900 instruction set.

7.2.1.2.1.4 Software Development Support - Intel provides the Series 3000 Cross Microprogramming System, CROMIS. It is available in ANSI (standard) FORTRAN IV source form for user installation or may be immediately accessed on any of several time sharing services. CROMIS basically provides a symbolic microassembler.

Raytheon provides the RAYASM symbolic microassembler for the 2900 family. It is available for immediate access on a time sharing service. In addition, Advanced Micro Devices provides the AMDASM symbolic microprogram assembler for the 2900 family.

TABLE 7-6. BIT SLICE MICROPROCESSOR COMPONENTS  
REQUIRED FOR IMPLEMENTING FRAMING UNIT

PRIMARY VENDOR	BIT-SLICE MICROPROCESSOR FAMILY	CHIPS REQUIRED TO IMPLEMENT AN 8-BIT FRAMING UNIT MICROCONTROLLER	
		QUANTITY	CHIP DESCRIPTION AND TYPE NO.
ADVANCED MICRO DEVICES	2900	2	2901 4-Bit Microprocessor Slice
		2	2909 4-Bit Microprogram Sequencer
FAIRCHILD	9400	2	9404 4-Bit Data Path Switch
		2	9405A 4-Bit Arithmetic Logic Register Stack
		2	9408 4-Bit Microprogram Sequencer
		2	9410 16 Word x 4-Bit Register Stack
		2	9407 4-Bit Data Access Register
INTEL	3000	1	3001 Microprogram Control Unit
		4	3002 Central Processing Element



In addition, the RAPID symbolic microprogram assembler is available on time sharing service and may be used for both the 2900 and 3000 families.

7.2.1.2.1.5 Cost - The cost of the 2900 and 3000 chips required to implement the Framing Unit Microcontroller is shown in Table 7-7. The cost of the 2900 chip set is slightly lower than the cost of the 3000 chip set.

TABLE 7-7. COMPARISON OF 2900 AND 3000 FAMILY CHIP COSTS

CHIP TYPE NUMBER ①	QUANTITY REQUIRED ②	COST PER CHIP ③	TOTAL CHIP COST PER FRAMING UNIT MICROCONTROLLER
2901DC	2	14.70	29.40
2909DC	2	8.50	17.00
3001DC	1	13.35	13.35
3002DC	4	8.80	35.20
			46.40
			48.55

- NOTES: ① Ceramic hermetic dip package
- ② Quantity required to implement one Framing Unit Microcontroller.
- ③ Quantity of 100-999 as of 24 March 1977.

7.2.1.2.6 Summary - The selection of a bit-slice microprocessor family narrowed to a choice between the Advanced Micro Devices 2900 family and the Intel 3000 family.

The 2900 family has a definite advantage in the areas of:

- Number of bits per slice
- Technical Parameters
- Number of chips required to implement the Framing Unit Microcontroller.

In addition, the 2900 has a slight edge in the area of software support in that three microprogram assemblers are available to choose from versus two for the 3000 family. In the area of chip

cost, the 2900 family has a slight advantage. The 2900 has an additional advantage in that it has a total of 5 sources including Advanced Micro Devices, while the 3000 has only two sources including Intel.

Taken the many advantages of the 2900 into account, it was selected to be utilized in the Framing Unit Microcontroller.

### 7.2.2 Hardware Specification

#### 7.2.2.1 Interface and Reassignment Group A (IRGA)

A block diagram of the IRGA is shown in Figure 7-2.

The IRGA has the following functional capabilities:

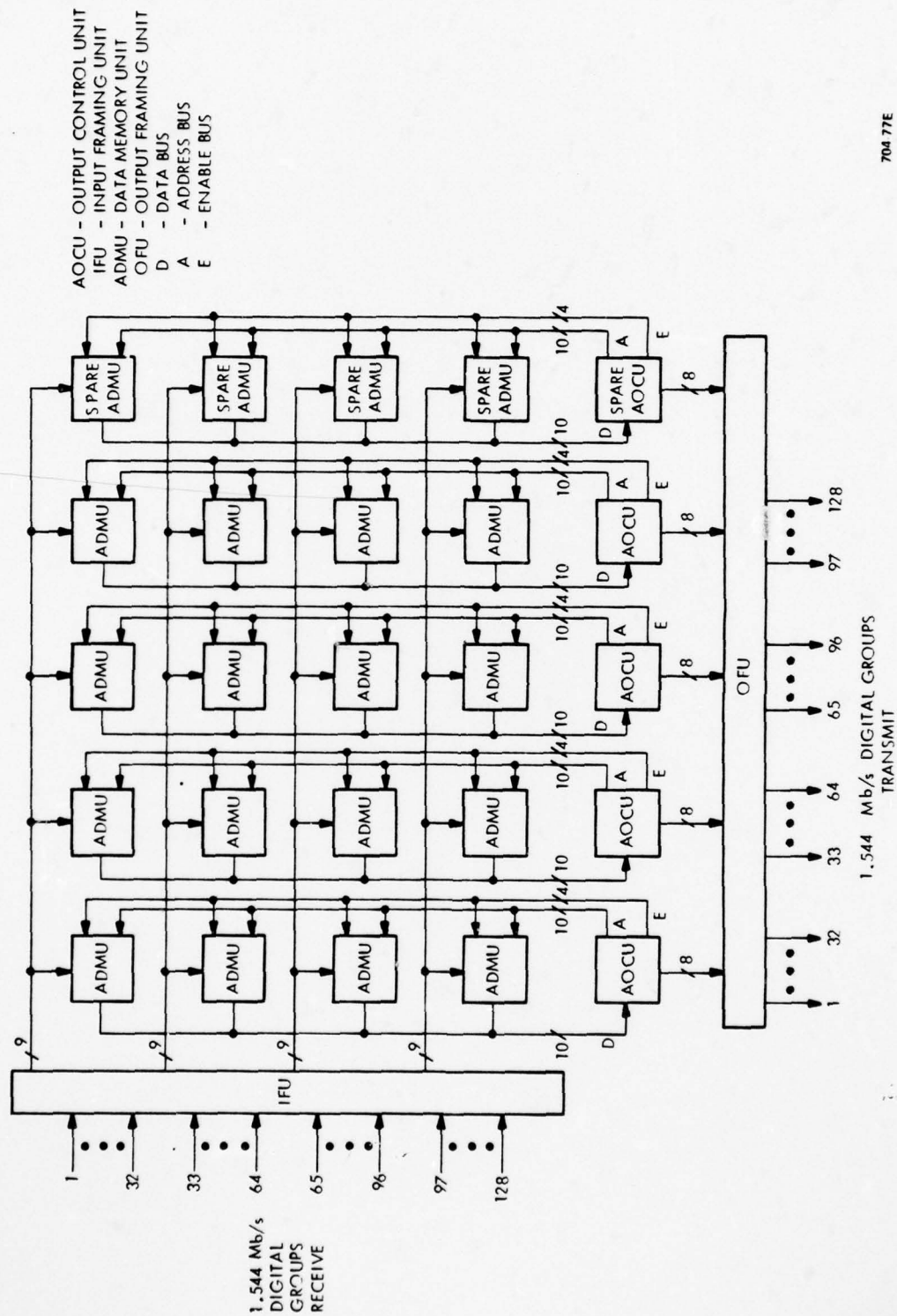
- a. Provides the traffic interfaces to the TD-1192 and the TD-1193 DRAMA multiplexers. The interface is at the 1.544 Mb/s T1 digital group level.
- b. Performs digital group channel reassignment.
- c. Permits loopback of the digital groups in either direction.
- d. Permits injection and extraction (monitoring) of T1 digital groups.
- e. Permits loopback at the digital group channel level in either direction.
- f. Provides BITE and performs fault isolation in conjunction with the Central Control Unit in the Common Equipment Group.

The IRGA comprises four basic functional hardware units:

1. Input Framing Unit (IFU)
2. A Data Memory Unit (ADMU)
3. A Output Control Unit (AOCU)
4. Output Framing Unit (OFU).

The IFU and OFU provide the basic function of interfacing the T1 digital groups from and to the DCS. The ADMUs and AOCUs provide the basic channel reassignment function under the control of the Central Control Unit (CCU) in the Common Equipment Group (CEG). The following sections provide details of each IRGA unit.

The IRGA is modularly expandable up to 192 digital group inputs in increments of 32 digital groups. Table 7-8 provides the IRGA printed circuit card requirements for each IRGA unit versus the number of 1.544 Mb/s digital group inputs.



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NOTE: CONFIGURED FOR A MAXIMUM OF 128 DIGITAL GROUPS

Figure 7-2. Interface and Reassignment Group A



TABLE 7-8. DEC IRGA CARD REQUIREMENTS VERSUS NUMBER OF 1.544 MB/S DIGITAL GROUP INPUTS

NUMBER OF DIGITAL GROUP INPUTS	NUMBER OF IFU CARDS REQUIRED	NUMBER <sup>1</sup> OF DMU CARDS REQUIRED	NUMBER <sup>1</sup> OF OCU CARDS REQUIRED	NUMBER OF OFU CARDS REQUIRED	TOTAL NUMBER OF IRGA CARDS
32	23	2	4	6	35
64	41	6	6	10	63
96	62	12	8	15	97
128	80	20	10	19	129
160	98	30	12	24	164
192	119	42	14	28	203

1. INCLUDES SPARES

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Figure 7-3 illustrates the 32 digroup IRGA in more detail. The number, size, and types of printed circuit cards are shown for each unit of the IRGA. Also shown are the signal and control lines between the units. Figure 7-4 is a hardware family tree of the IRGA.

7.2.2.1.1 Input Framing Unit (IFU) - The IFU accepts 1.544 Mb/s T1 digital groups from a TD-1192, TD-1193, another DCE or from the IRGB. With respect to the digital groups received from a TD-1192, TD-1193 or another DCE, the IFU provides:

- a. Elastic FIFO buffering to maintain BCI
- b. Frame acquisition and maintenance
- c. Master frame alignment of all digital groups to an internal DCE frame reference
- d. Conversion of digital groups from serial to parallel format on a per channel basis (8 bits). A ninth parity bit is appended to each 8-bit channel.
- e. Time multiplexing of 32 digital groups (in parallel format) for passage to the IRGA time division matrix for reassignment. Up to 32 digital groups are multiplexed together. 192 groups are handled by breaking them into 5 groups of 32.

7.2.2.1.1.1 IFU Hardware Description and Operation - The IFU is modularly configured and may handle up to a maximum of 192 T1 digital group inputs. A detailed block diagram of the IFU is provided in Figure 7-5.

The IFU consists of the following hardware elements:

- a. Digital Group Buffer
- b. Frame Alignment Buffer
- c. Framing Unit
- d. Serial to Parallel Converter
- e. Parity Generator
- f. Digital Group Multiplexer
- g. Multiplexer Controller.

These hardware elements are described in detail below.

- a. Digital Group Buffer - The IFU will provide a Digital Group Buffer for each digital group terminating at the DCE IRGA. These buffers compensate for transmission variations and timing differences between the DCE Master Timing Unit and the 1.544 MHz clock for each digital group. In Section 6.4.2, it is shown that a 206-bit buffer is required. The Digital Group Buffer is a 256-bit FIFO elastic buffer.

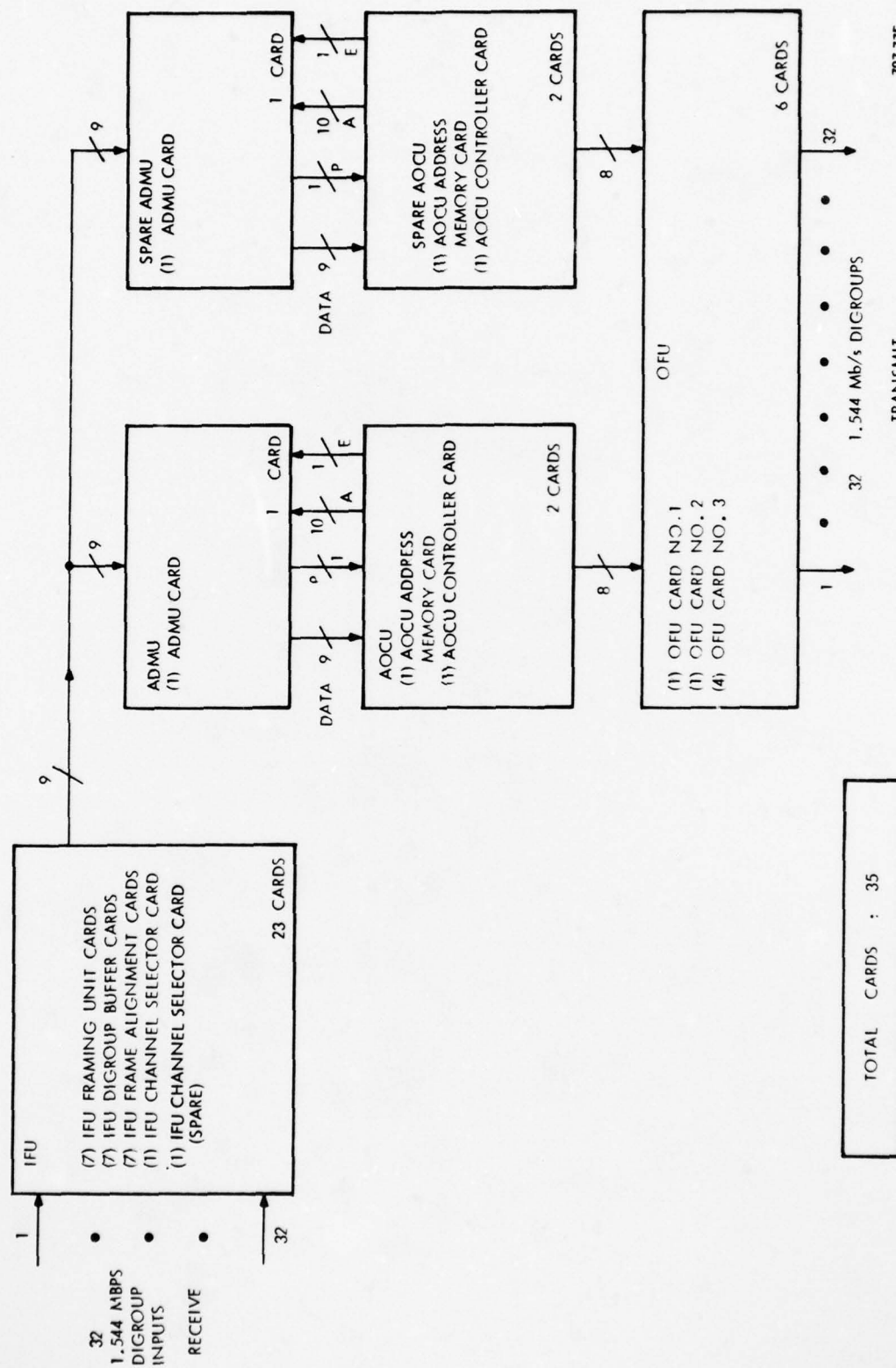


Figure 7-3. DCE IRGA - 32 Digital Group Size



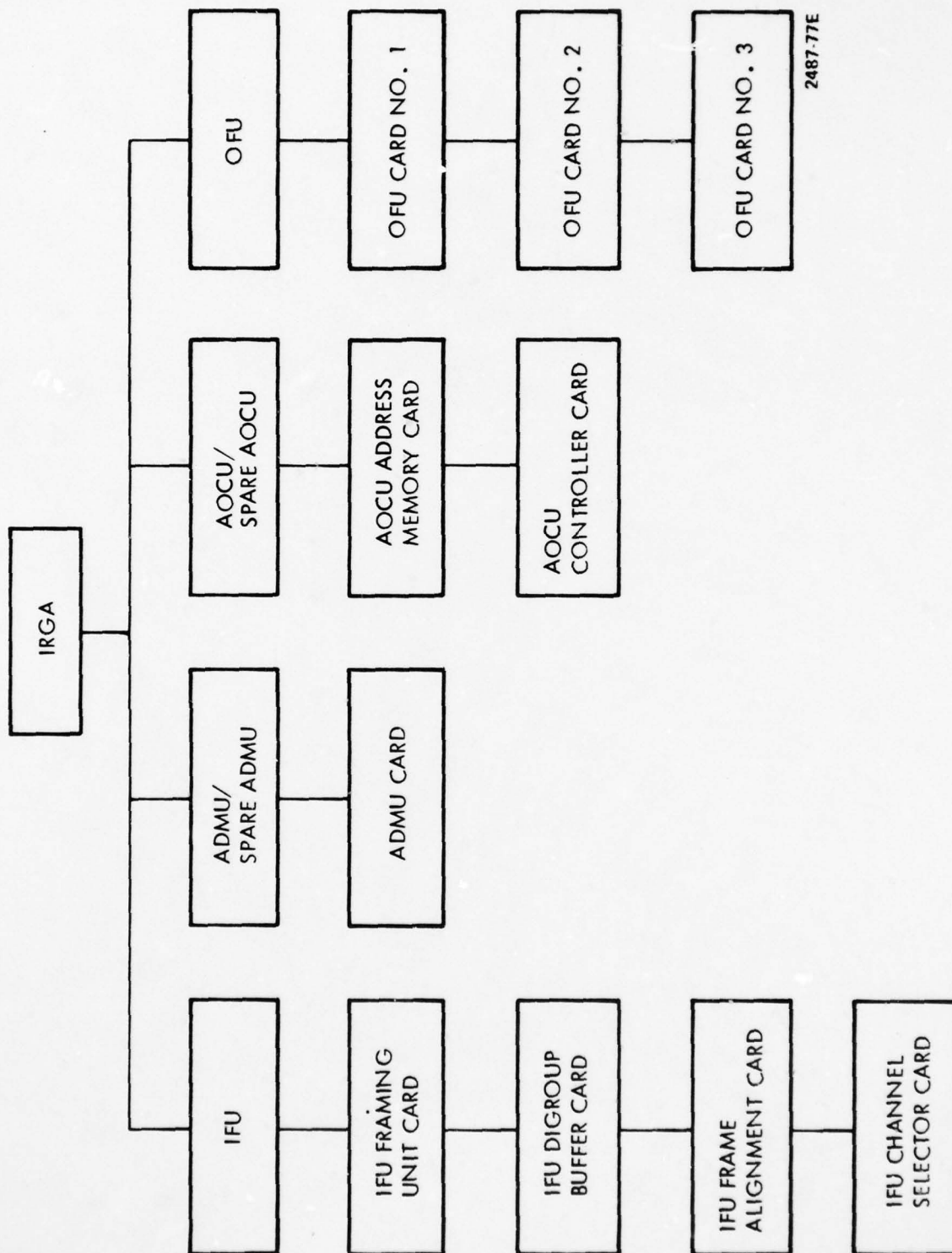


Figure 7-4. IRGA Hardware Family Tree

AD-A071 672

GTE SYLVANIA INC NEEDHAM HEIGHTS MASS ELECTRONIC SYS--ETC F/G 17/2  
DIGITAL NETWORK CONTROL.(U)  
MAY 77

UNCLASSIFIED

SBIE -AD-E100 237 DCA100-76-C-0064  
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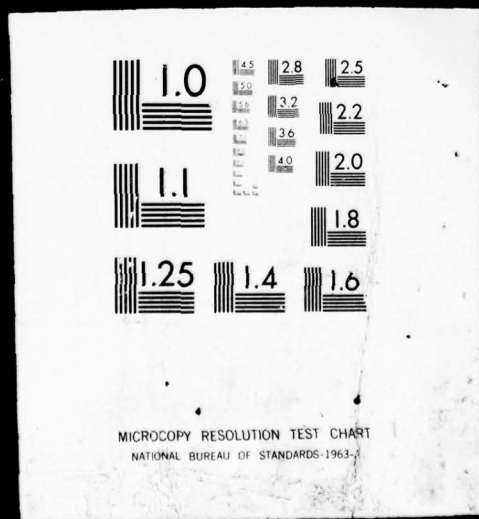
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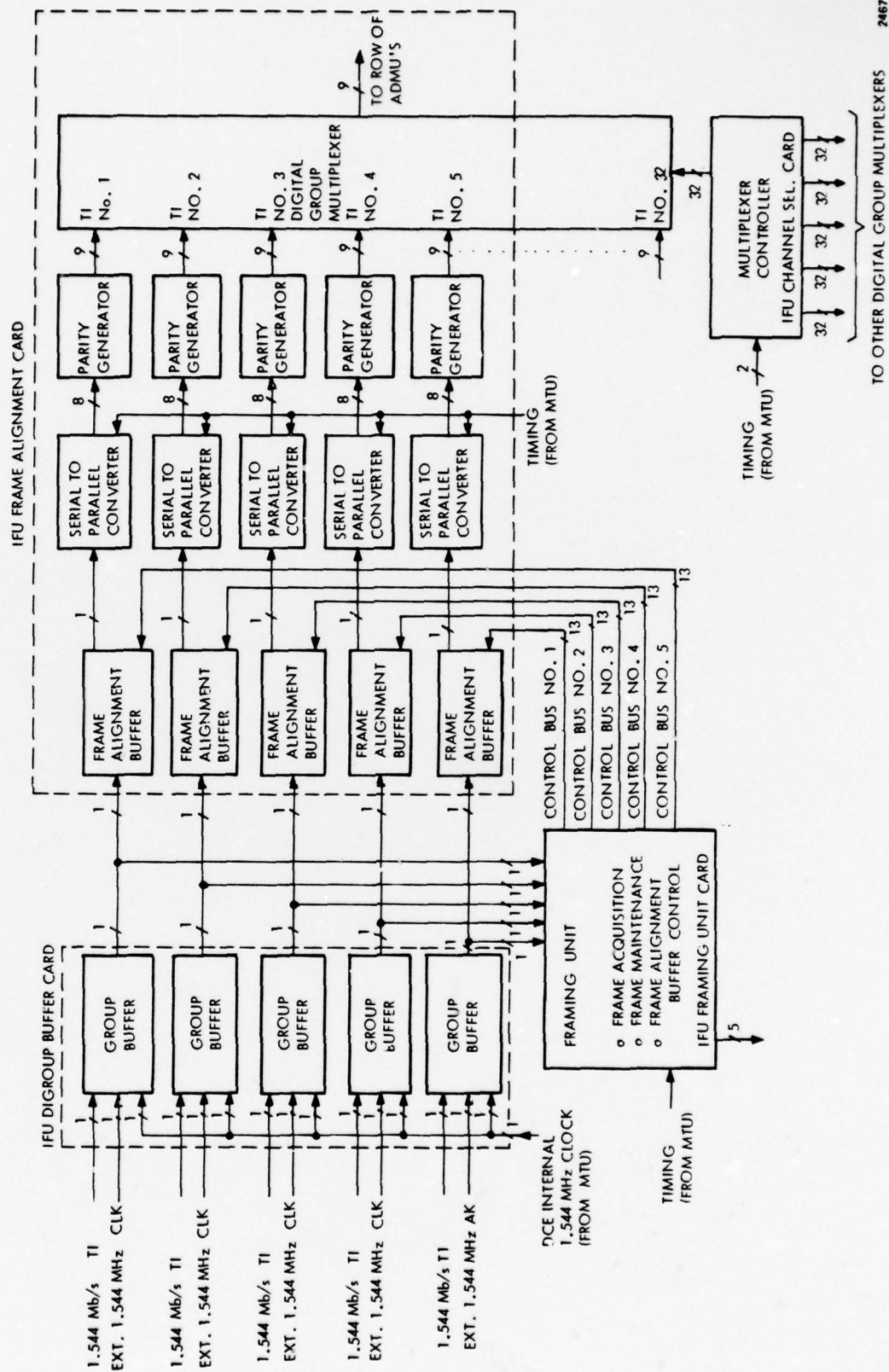


Figure 7-5. Input Framing Unit Block Diagram

- b. Frame Alignment Buffer - A frame alignment buffer is provided for each T1 input digital group. This buffer has a capacity of 6 T1 frames (1158 bits). Under the control of the Framing Unit Microcontroller, these buffers align all the input T1 digital groups on a six-frame basis to an internal DCE frame reference.
- c. Framing Unit - This hardware element services up to five T1 digital group inputs. It performs T1 frame acquisition and maintenance for each T1 group, detection of loss of frame synchronization and control of five Frame Alignment Buffers. The Framing Unit has a status interface with the Central Control Unit (CCU) in the Common Equipment Group. It reports the frame synchronization status of each T1 digital group that it services.
- d. Serial to Parallel Converter - The digital groups terminating at the DCE IRGA are in serial format. Each terminating digital group is passed through a Serial to Parallel Converter and becomes a parallel format digital group. The conversion is done 8 bits at a time and is accomplished in such a way that each 8-bit serial channel in a digital group is converted to an 8-bit parallel channel.
- e. Parity Generator - The Parity Generator adds a 9th parity bit to each 8-bit parallel digital group channel from the Serial to Parallel Converter. This parity bit is such that the entire 9-bit parallel word exhibits odd parity.
- f. Digital Group Multiplexer - The Digital Group Multiplexer accepts 32 T1 digital groups (in 8-bit parallel format with a 9th parity bit) and multiplexes them into a parallel 6.176 MHz data stream. During the 192 channel bit times of a T1 frame, 768 9-bit parallel channel words are output by the Multiplexer. There is no output from the Multiplexer during the 193rd T1 frame bit time. Six Digital Group Multiplexers are required for 192 input digital group.
- g. Multiplexer Controller - The Multiplexer Controller provides a sequence of enable signals to the Digital Group Multiplexer such that all 32 T1 digital groups are properly multiplexed together.

7.2.2.1.1.2 Partitioning of IFU Hardware Elements - The IFU is designed to be modularly expandable in increments of five terminating digital groups. To accomplish this, the IFU hardware is partitioned onto four printed circuit card types as follows (see Figure 7-5 also):

- |    |                            |   |           |
|----|----------------------------|---|-----------|
| a. | IFU Framing Unit Card      | } | Basic IFU |
| b. | IFU Digroup Buffer Card    |   | Modular   |
| c. | IFU Frame Alignment Card   |   | Element   |
| d. | IFU Channel Selector Card. |   |           |

Referring to Figure 7-5, 1.544 Mb/s digital groups from the IRGB are directly input to the IFU Frame Alignment Card. The IFU Framing Unit and Digroup Buffer Cards are not required for digital groups from the IRGB.

With the exception of the IFU Channel Selector Card, each card type is designed to service five digital groups. The IFU Channel Selector Card services up to the maximum number of input digroups (192). Therefore, the basic IFU modular element for five input digital groups consists of three printed circuit cards. Table 7-9 indicates the number of each card type versus the basic DCE IRGA size in increments of 32 digital group inputs.

Referring to Figure 7-5, the IFU hardware functions are partitioned among the four IFU card types as follows:

- a. IFU Framing Unit Card - This card contains one Framing Unit.
- b. IFU Digroup Buffer Card - This card contains five Digital Group Buffers.
- c. IFU Frame Alignment Card - This card contains five Frame Alignment Buffers (6 frames), five Serial to Parallel Converters, five Parity Generators and a portion of the Digital Group Multiplexer.
- d. IFU Channel Selector Card - This card contains the Multiplexer Controller hardware. It controls up to six Digital Group Multiplexers. A redundant card is provided and either card may be placed in service under the control of the CCU.



TABLE 7-9. IFU CARD REQUIREMENTS VERSUS IRGA SIZE

IRGA SIZE IN NUMBER OF DIGITAL GROUPS	IFU FRAMING UNIT CARD	IFU DIGROUP BUFFER CARD	IFU FRAME ALIGNMENT CARD	IFU CHANNEL SELECTOR CARD	TOTAL NUMBER OF IFU CARDS
32	7	7	7	2 See Note 1	23
64	13	13	13	2 See Note 1	41
96	20	20	20	2 See Note 1	62
128	26	26	26	2 See Note 1	80
160	32	32	32	2 See Note 1	98
192	39	39	39	2 See Note 1	119

Note: 1. A redundant IFU Channel Selector Card is included in this total.

7.2.2.1.2 IRGA Time Division Memory Matrix - The IRGA Time Division Memory Matrix is made up of A Data Memory Units (ADMU). The number of ADMUs required depends on the size of the IRGA. Figure 7-5A illustrates the IRGA Time Division Memory Matrix for each size IRGA in increments of 32 digital groups. The matrix is modular in increments of 32 digital groups up to a maximum of 192 digital groups. As discussed later, each ADMU consists of one printed circuit card. For each size Time Division Memory Matrix, one column of ADMUs is a spare column. The spare column of ADMUs is on hot standby and can be switched into service by the Central Control Unit to replace a column which has a failed ADMU. Depending on the matrix size, the number of spare ADMUs range from one to six. All ADMUs are identical, including the spares.

The IRGA Time Division Memory Matrix plus the A Output Control Units (AOCUs) provide the IRGA digital time division switching capability. Data from the Data Input Bus is written into all the ADMUs in a row and data is read out from the ADMUs onto the Output Data Bus by the AOCUs, accomplishing the switching function.

The theory of the Time Division Switching approach, which is used in the IRGA, is discussed in detail in Section 5.2.2, Digital Time Division Switching. Some additional details of the operation of the IRGA Time Division Memory Matrix are provided in Section 6.2.1.1, IRGA.

The following section provides the details of the hardware implementation of the ADMU which is the basic element of the IRGA Time Division Memory Matrix.

7.2.2.1.2.1 ADMU Hardware Description - The ADMU is the heart of the IRGA Time Division Memory Matrix in that it is the element that performs the reassignment of individual T1 8-bit channels and entire digital group. Each ADMU has 32 digroups input to it in a time-multiplexed format from the IFU.

A detailed block diagram of the ADMU is provided in Figure 7-6. The ADMU consists of the following hardware elements:

- a. Data Memory No. 1 is a 768 x 9 bit random access memory (RAM).
- b. Data Memory No. 2 is a 768 x 9 bit RAM.
- c. A controller which determines whether a Data Memory is in the read or write mode and provides the correct addresses to the Data Memories. The Controller interfaces with the A Output Control Unit (AOCU).

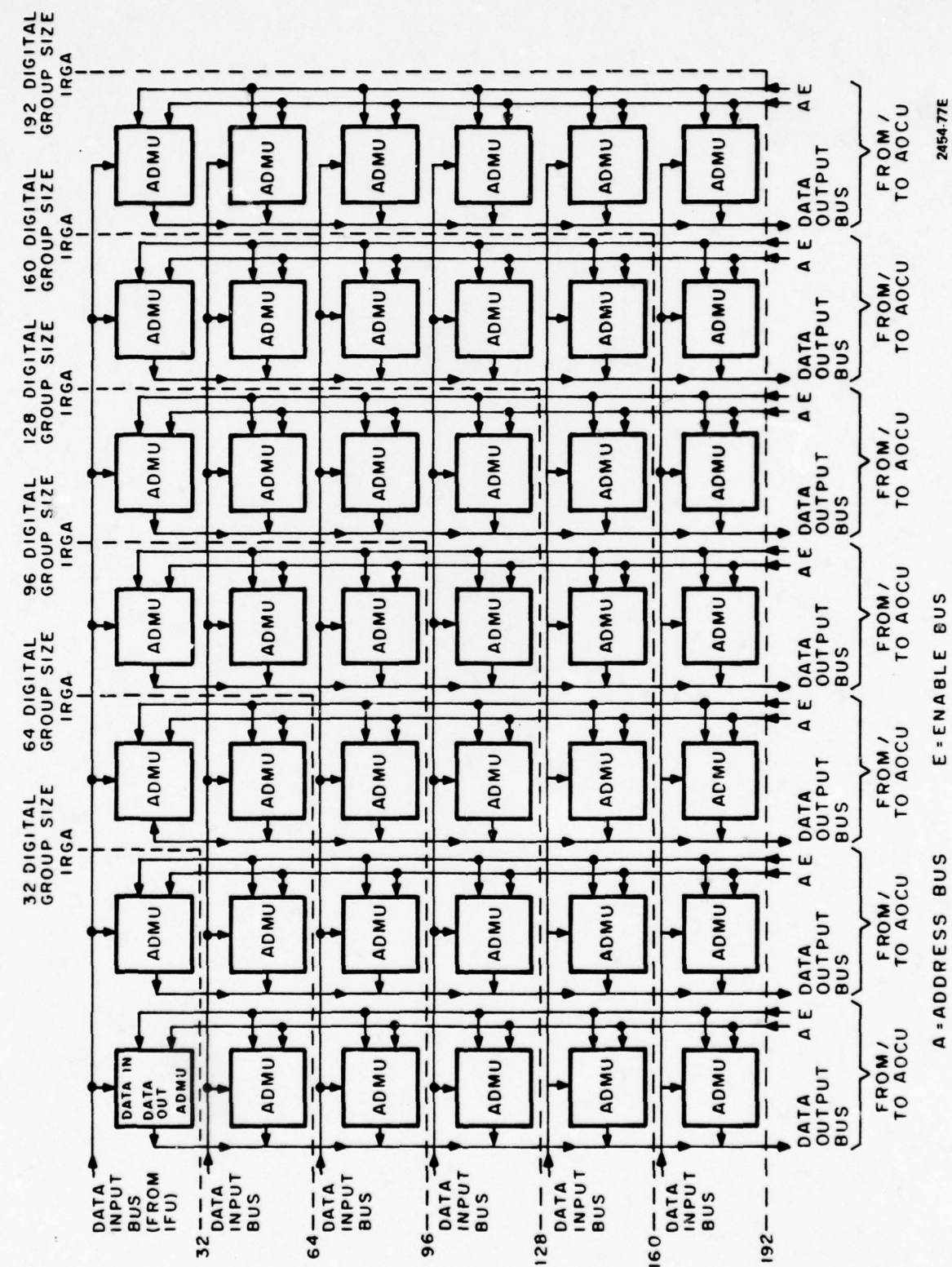
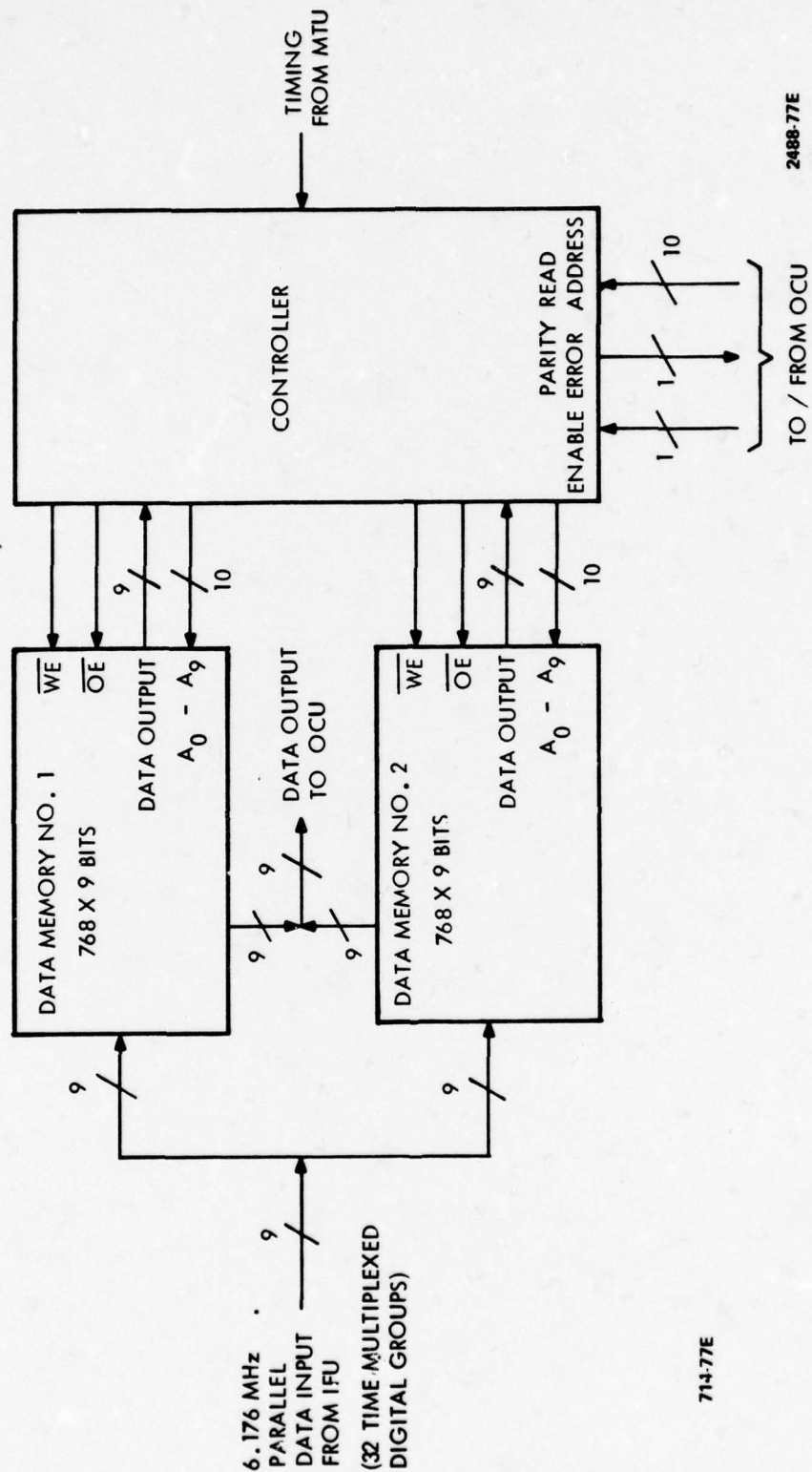


Figure 7-5A. IRGA Time Division Memory Matrix

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Figure 7-6. A Data Memory Unit Block Diagram

7.2.2.1.2.2 ADMU Hardware Operation - Figure 7-7 illustrates the frame structure of a 1.544 Mb/s T1 digital group. Figure 7-8 illustrates a portion of the 9-bit parallel data stream (6.176 MHz) input to the ADMU from the IFU. This parallel data stream contains 32 digroups. The digroup channels are in 8-bit parallel format with a 9th parity bit added. In one T1 bit time (648 ns), are four 8-bit parallel channels each from a different digroup. Thus, in one channel time (5.184  $\mu$ s) there are 32 digroup channels. It is important to note, as shown in Figure 7-8, that during the channel 5 time in a serial frame, 32 different parallel digroup channel 5s are multiplexed together.

Figure 7-9 illustrates the operation of the ADMU. During the 192 T1 bit times, one Data Memory is placed in the read mode while the other data memory is placed in the write mode. The Data Memory in the write mode, writes  $32 \times 24 = 768$  9-bit digroup channels into RAM during 192 bits of the T1 frame. The Data Memory in the read mode reads  $32 \times 24 = 768$  9-bit digroup channels out of RAM during 192 bits of the T1 frame. This read Data Memory also checks the parity of each channel and reports parity errors to the CCU via the AOCU. The sequence of reading out of the Data Memory is controlled by the AOCU which provides 768 read addresses to the ADMU controller. The basic feature of channel reassignment resides in the sequence that channels are read out of the data memory.

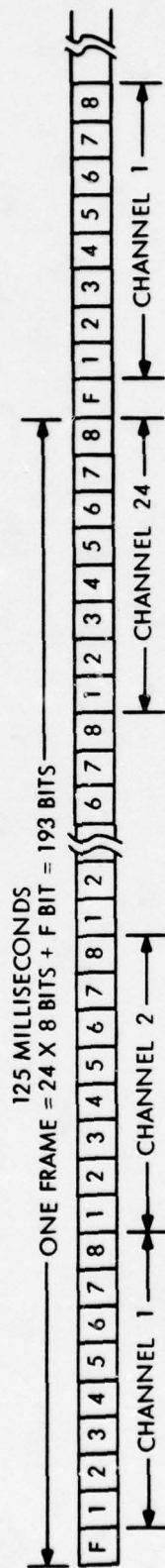
During the frame bit time (bit 193, 648 ns), the modes of the data memories are switched. Thus, in the next T1 frame, the read mode data memory becomes the write mode data memory and the write mode data memory becomes the read mode data memory. As shown in Figure 7-9, during each T1 frame, one data memory is always reading data out, while the other data memory is always writing data in.

7.2.2.1.2.3 ADMU Hardware Alternatives - There is a speed constraint on the data memory (RAM). This constraint placed a maximum limit on the duration of a read or write cycle. This time is given by:

$$T_R \text{ or } W \leq \frac{n}{R \left( \left\lceil \frac{N}{D} \right\rceil + I \right)} \quad (7-1)$$

$$\left\lceil x \right\rceil = \text{Smallest integer } \geq x$$

$T_R \text{ or } W$  = Memory cycle time, seconds  
Cycle



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BIT TIME = 648 NANOSECONDS  
 CHANNEL TIME = 5.184 MICROSECONDS  
 (8 BITS)

Figure 7-7. Frame Structure of a 1.544 Mb/s T1 Digital Group



DIGROUP CHANNEL 5																																		
BIT 7				BIT 6				BIT 5				BIT 4				BIT 3				BIT 2				BIT 1				BIT 0						
162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	162	
NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	

DIGRP #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6	B6
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5	B5
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P

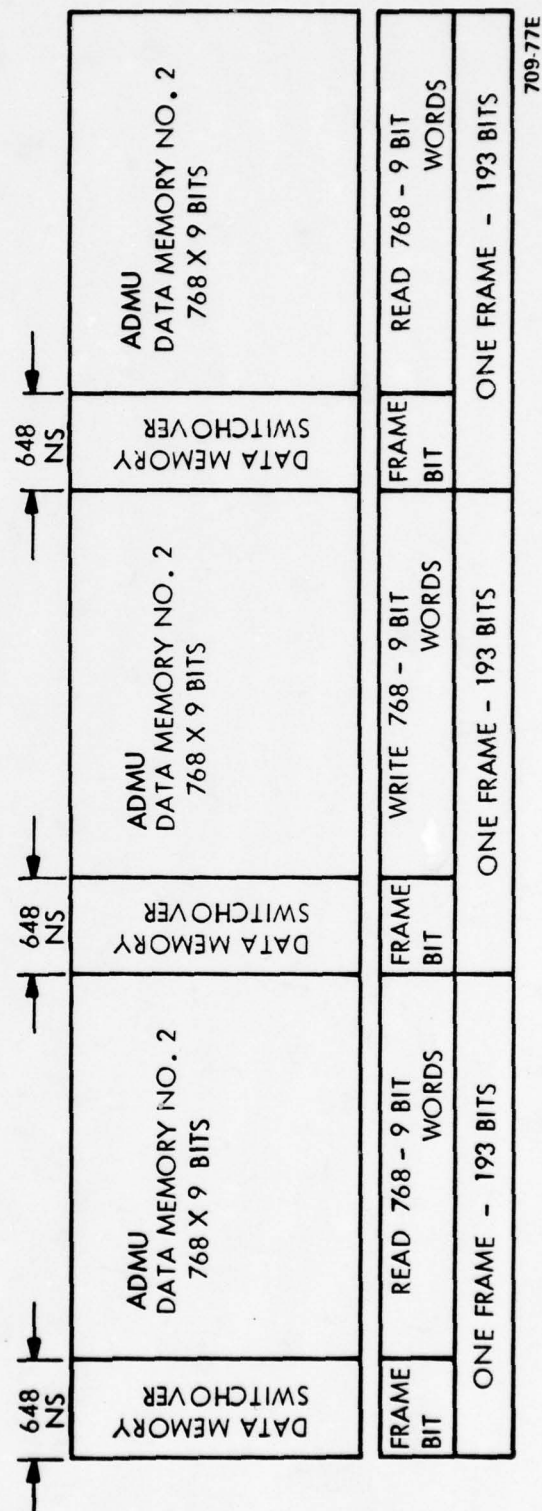
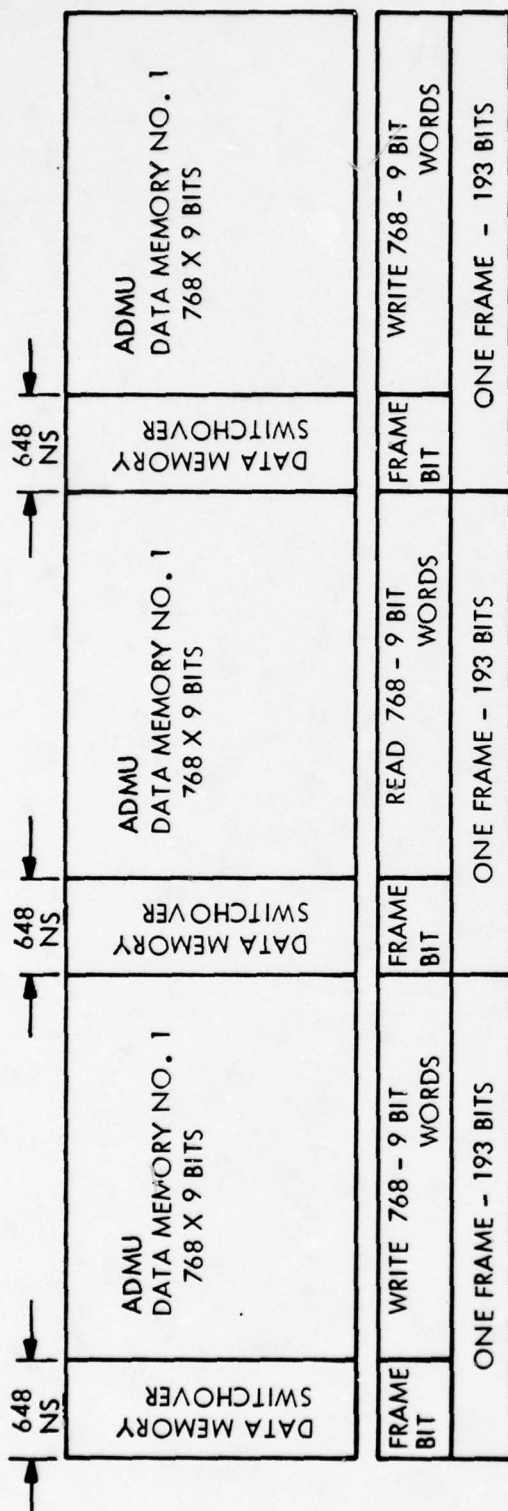
DIGROUP #1/CH.5

DIGROUP #2/CH.5

DIGROUP #32/CH.5

720 77E

Figure 7-8. DMU Data Input From IFU



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Figure 7-9. Data Memory Unit (DMU) Operation

- n = Number of bits transferred per access
- R = Group data rate, bits/second
- N = Number of groups
- D = Redundancy factor (number of copies of data memory, not counting double buffering)
- I =  $\begin{cases} 0 & \text{If double buffered} \\ \text{Number of serial writes if not double buffered} \end{cases}$

The first alternative considered was to determine the number of bits to be transferred per access. The T1 format of 8 bits per channel lends itself to 8-bit transfers per data memory access. In addition, transfers of less than 8 bits results in a very high redundancy factor (D) to keep the data memory speed constraint within a range which can be readily achieved with current RAM ICs. Also, transferring 8 bits per data memory access, results in simplified data memory controller circuit logic.

The second alternative considered was the use of double buffering. Double buffering means that two data memories are used instead of one in an ADMU. These are simultaneously read from and written into. Double buffering was selected to obtain a low redundancy factor and maintain an achievable data memory speed constraint.

The third alternative considered was the selection of an optimum redundancy factor and the selection of optimum RAM ICs to implement the data memories. Substituting  $R=1.544 \text{ Mb/s}$ ,  $n=8$  and  $I=0$  into Equation 7-1 we get:

$$\begin{array}{l} T_R \text{ or } W \leq \frac{5.181 \text{ } \mu\text{S}}{\left[ \frac{N}{D} \right]} \\ \text{Cycle} \end{array} \quad (7-2)$$

The IRGA will be configured modularly up to a maximum size of  $N=192$  1.544 Mb/s T1 digroups. Using Equation 7-2 and  $N=192$ , we can determine the data memory speed constraint versus the redundancy factor (D). The basic IRGA modularity is given by  $[N/D]$  digroups. Table 7-10 summarizes this information. Table 7-11 presents the candidate RAM ICs and technologies considered for implementing the ADMU data memories.



TABLE 7-10. DATA MEMORY CONSTRAINTS VERSUS  
IRGA MODULARITY

REDUNDANCY FACTOR, D	$T_R$ OR $W \leq$ CYCLE CONSTRAINT	IRGA MODULARITY SIZE: # OF INPUT DIGITAL GROUPS	DATA MEMORY SIZE	RAM CHIP ACCESS TIME $\leq$	CANDIDATE RAM CHIP TECHNOLOGIES
2	56 ns	92	2208 x 9 Bits	28 ns	ECL
3	81 ns	64	1536 x 9 Bits	40 ns	ECL
4	108 ns	48	1152 x 9 Bits	51 ns	ECL
5	130 ns	40	960 x 9 Bits	65 ns	ECL, TTL
6	162 ns	32	768 x 9 Bits	81 ns	TTL, LPTTL
7	185 ns	28	672 x 9 Bits	92 ns	TTL, LPTTL
8	216	24	576 x 9 Bits	108 ns	TTL, LPTTL
9	236	22	528 x 9 Bits	118 ns	TTL, LPTTL
10	259 ns	20	480 x 9 Bits	129 ns	TTL, LPTTL
11	288 ns	18	432 x 9 Bits	144 ns	TTL, LPTTL
12	324 ns	16	384 x 9 Bits	162 ns	TTL, LPTTL NMOS, CMOS
14	370	14	336 x 9 Bits	185 ns	TTL, LPTTL NMOS, CMOS
16	432 ns	12	312 x 9 Bits	216 ns	TTL, LPTTL NMOS, CMOS
20	518 ns	10	240 x 9 Bits	259 ns	TTL, LPTTL NMOS, CMOS

Good design practice dictates that a RAM IC should have a maximum access time of one-half of the maximum cycle time constraint given by Equation 7-2. The major goal in the selection process is to achieve the lowest redundancy factor (D) consistent with a readily achievable  $T_R$  or  $W/CYCLE$  using commercially available RAM ICs. The second objective is to minimize the number of RAM IC packages required to implement a data memory. This objective dictates that fairly dense RAMs be used. Finally, a reasonable modularity is required.

TABLE 7-11. CANDIDATE RAM ICs AND TECHNOLOGIES CONSIDERED FOR IMPLEMENTING THE ADMU DATA MEMORIES

NO.	ORGANIZATION	TECHNOLOGY	COMMENTS
1	64 x 9 Bit	TTL	Permits Low DMU Redundancy
2	256 x 1 Bit	TTL - Low Power	Low Bit Density Useful for Storing Parity Bit
3	256 x 4 Bit	TTL - Low Power	Permits Low DMU Redundancy
4	256 x 4 Bit	NMOS	Requires High DMU Redundancy
5	256 x 4 Bit	CMOS	Requires High DMU Redundancy
6	1024 x 1 Bit	TTL	Poor DCE Modularity Results

After evaluating all of the above data against the design objectives, a redundancy factor of 6 was chosen. This provides a modularity of 32 digroups. The data memory specifications based on a redundancy factor of 6 are as follows:

a.  $T_R$  OR  $W \leq 162$  ns  
CYCLE

b. Size: 768 x 9 Bits

$$(768 = 32 \times 24)$$

NUMBER  
OF  
DIGROUPS

NUMBER  
OF CHANNELS  
PER FRAME

TABLE 7-12. COMPARISON OF DATA MEMORY IMPLEMENTATIONS

IMPLEMENTATION	IC RAM TYPE(S)	NO. OF IC'S PER ADMU	NO. OF IC'S PER 42 ADMUS (3)	MAXIMUM PWR. DISS. IN mw/BIT	MAXIMUM PWR. DISS. (W) PER 42 ADMUS (3)
A (Preferred)	256 x 4 (1)	12	504	0.391	202
	256 x 1 (1)	6	252	1.367	88
	Totals	18	756	0.499 (2)	290
B	64 x 9 (1)	24	1008	1.736	1008

NOTES: (1) 256 x 4 = 93L422DC  
 256 x 1 = 93L420DC  
 64 x 9 = 93419DC

(2) Weighted Average

(3) 42 ADMUS are required to service 192 input digital groups. 6 of these are spare (hot standby) ADMUS.



There are two hardware alternatives to implement the data memory. These alternatives are illustrated in Figure 7-10. Table 7-12 provides a comparison of these alternatives. The preferred alternative is implementation A. It requires fewer RAM IC packages and provides a significant reduction in power dissipation over the B implementation. The cost of the ICs for implementation B is approximately 116 percent higher than the cost of ICs for the preferred approach. This is based on the number of ICs required to populate 42 ADMUs.

7.2.2.1.2.4 Partitioning of ADMU Hardware Functions - The ADMU hardware functions, namely:

- a. Data Memory No. 1
- b. Data Memory No. 2
- c. Controller.

will be packaged on one printed circuit card. Table 7-13 indicates the number of ADMU cards versus the size of the IRGA.

TABLE 7-13. ADMU CARD REQUIREMENTS VERSUS IRGA SIZE

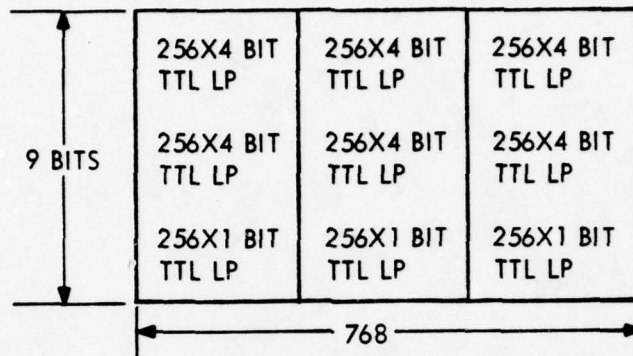
IRGA SIZE (DIGITAL GROUPS)	NUMBER OF ADMU CARDS REQUIRED ①
32	2
64	6
96	12
128	20
160	30
192	42

NOTE: ① This includes spare ADMU cards.

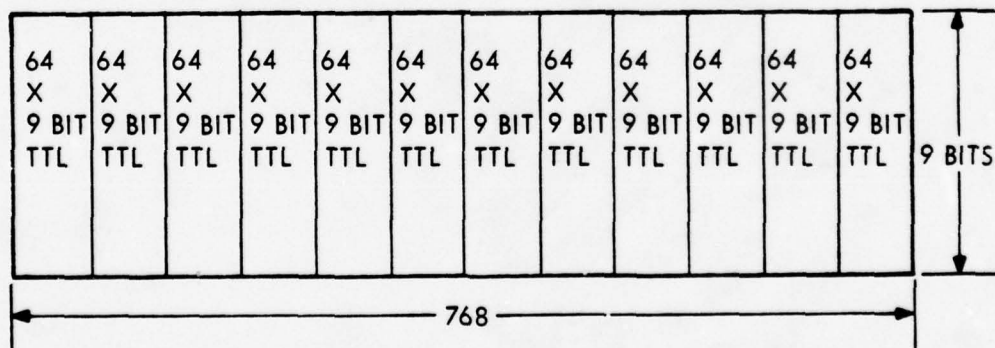
7.2.2.1.3 A Output Control Unit (AOCU)

7.2.2.1.3.1 AOCU Hardware Description and Operation - The AOCU controls the ADMUs to perform channel reassignment. The AOCU interfaces directly with the Central Control Unit (CCU) in the Common Equipment Group (CEG).

### DATA MEMORY IMPLEMENTATION A



### DATA MEMORY IMPLEMENTATION B



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Figure 7-10. ADMU Data Memory Hardware Implementation Alternatives

A detailed block diagram of the AOCU is provided in Figure 7-11. The AOCU consists of the following hardware elements:

- a. Command Parity Check Function
- b. Address Memory
- c. Output Controller Function
- d. Address Memory Parity Check Function
- e. Data Memory Parity Check Encoder Function
- f. Connection Address Register
- g. Parity Status Register.

These functions are described in detail below.

- a. Command Parity Check Function - The CCU controls the AOCU via a 31-bit parallel command interface. CCU commands are received by the Command Parity Check Function. Figure 7-12 illustrates the various fields in the CCU command. The Command Parity Check Function checks the parity of the 31-bit command. If the 31-bits do not display odd parity, then the CDMP output is set to logic "1" and the CDMP status bit is set to a "1" in the Parity Status Register. Also, the command is inhibited from acting on other AOCU hardware by disabling the RCA' and WCA' outputs. The Command Parity Check Function also strips the CA and LOC fields off the command and sends these to the Address Memory and the Output Controller Function, respectively.
- b. Address Memory - The Address Memory is a 768 x 15-bit RAM. It stores 768 connection addresses (CA<sub>0</sub> - CA<sub>14</sub>). The connection address determines which ADMU in a column of ADMUs an AOCU will read from and which channel shall be read from the selected ADMU Data Memory. The channel reassignment function of the IRGA depends on the sequence in which connection addresses are stored in the Address Memory. The Address Memory performs a read access each 162 ns and 768 accesses are completed in one T1 frame (192 bits). The Address Memory may be written into or read from during the T1 frame bit time under the control of the CCU.
- c. Output Controller Function - The Output Controller Function provides a sequential address to the Address Memory (0 to 767) during the 192 channel bits of the T1 frame. During the T1 frame pulse, it can provide an address specified by the LOC field of the CCU command to



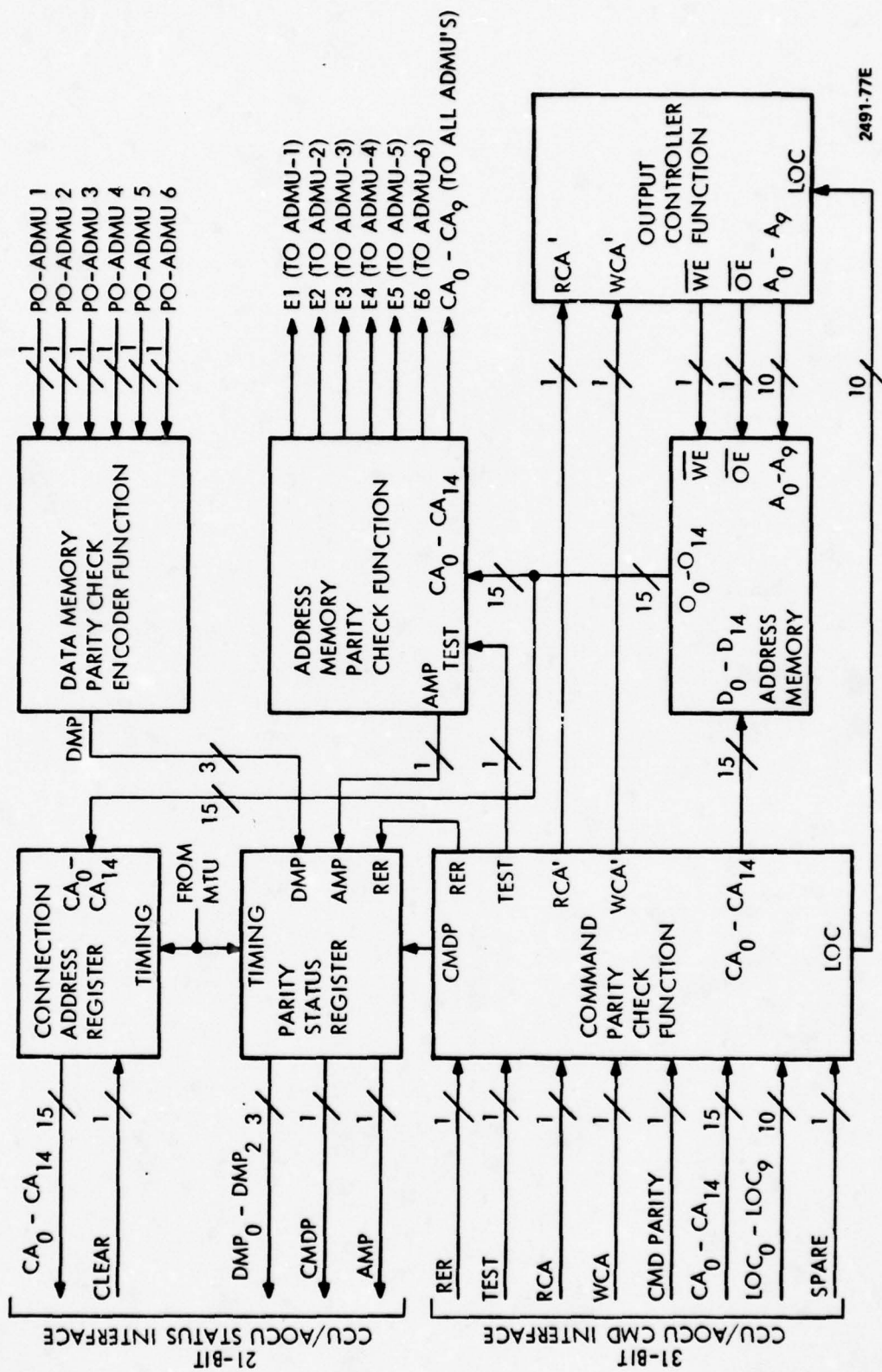


Figure 7-11. An Output Control Unit Block Diagram

COMMAND PARITY BIT		C	30	MSB
SPARE BIT		C	29	
LOC <sub>9</sub>		C	28	
LOC <sub>0</sub>		C	19	
CA <sub>14</sub>	CA PARITY BIT	C	18	
CA <sub>13</sub>	ADMU ENABLE CODE 4-BITS			
CA <sub>10</sub>				
CA <sub>9</sub>				
	ADMU DATA MEMORY READ ADDRESS 10-BITS			
CA <sub>0</sub>		C	4	
RER		C	3	
TEST		C	2	
RCA	READ CONNECTION ADDRESS	C	1	
WCA	WRITE CONNECTION ADDRESS	C	0	LSB

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Figure 7-12. CCU Command Format for AOCU Control

the Address Memory. The CCU command may specify the following actions on the Address Memory during the T1 frame bit time:

1. Read CA from Address Memory which is stored at address LOC.
2. Write CA into Address Memory at address LOC. Then read the contents of LOC.

In this way, the CCU can update the Address Memory or perform periodic tests on the Address Memory. In either case, the CA read from the Address Memory is clocked into the Connection Address Register.

- d. Address Memory Parity Check Function - Whenever a CA is read from the Address Memory, the Address Memory Parity Check Function checks the parity of the 15-bit CA. If the parity is not odd, the AMP output is set to a logic "1" which also sets the AMP status bit to a "1" in the Parity Status Register. Also, if the parity is bad, the CA is inhibited from being sent to any of the ADMUs. If the parity is odd, the Address Memory Parity Check Function strips off bit CA<sub>14</sub> and routes CA<sub>0</sub>-CA<sub>9</sub> to the ADMUs. It also decodes bits CA<sub>10</sub>-CA<sub>13</sub> to determine which ADMU is being addressed and sets the enable output for that ADMU to a logic "1".
- e. Data Memory Parity Check Encoder Function - Each ADMU Data Memory checks the parity of each 9-bit channel word which is read from it. If the parity is not odd, then it sets its PO output to a logic "1". The Data Memory Parity Check Encoder Function encodes which of the 6 ADMUs in a column is reporting PO="1". The encoding is done with three bits (DPM<sub>0</sub>-DMP<sub>2</sub>). These bits are sent to the Parity Status Register.
- f. Connection Address Register - This hardware element is a 15-bit storage register which stores the CA read from the Address Memory during a T1 frame bit time. It holds this CA until the CCU requires it. The CCU resets this register after it reads the CA from it by use of the CLEAR bit.
- g. Parity Status Register - The Parity Status Register is a 5-bit storage register which stores DMP<sub>0</sub>-DMP<sub>2</sub>, AMP and CMDP for reporting to the CCU. The CCU can reset this register to all "0's" by using the RER command bit.



7.2.2.1.3.2 Partitioning of AOCU Hardware Functions - The AOCU hardware functions will be packaged on two printed circuit cards. The two cards are as follows (see Figure 7-11 also):

- a. AOCU Controller Card
- b. AOCU Address Memory Card.

Table 7-14 indicates AOCU card requirements versus IRGA size.

7.2.2.1.3.2.1 AOCU Controller Card - The AOCU Controller Card contains the following hardware functions:

- a. Command Parity Check Function
- b. Output Controller Function
- c. Address Memory Parity Check Function
- d. Connection Address Register
- e. Parity Status Register.

7.2.2.1.3.2.2 AOCU Address Memory Card - This card contains the following hardware functions:

- a. Address Memory
- b. Data Memory Parity Check Encoder Function.

TABLE 7-14. AOCU CARD REQUIREMENTS VERSUS IRGA SIZE

IRGA SIZE (DIGITAL GROUPS)	NUMBER OF AOCU CONTROLLER CARDS REQUIRED ①	NUMBER OF AOCU ADDRESS MEMORY CARDS REQUIRED ①
32	2	2
64	3	3
96	4	4
128	5	5
160	6	6
192	7	7

NOTE: ① Includes spare card

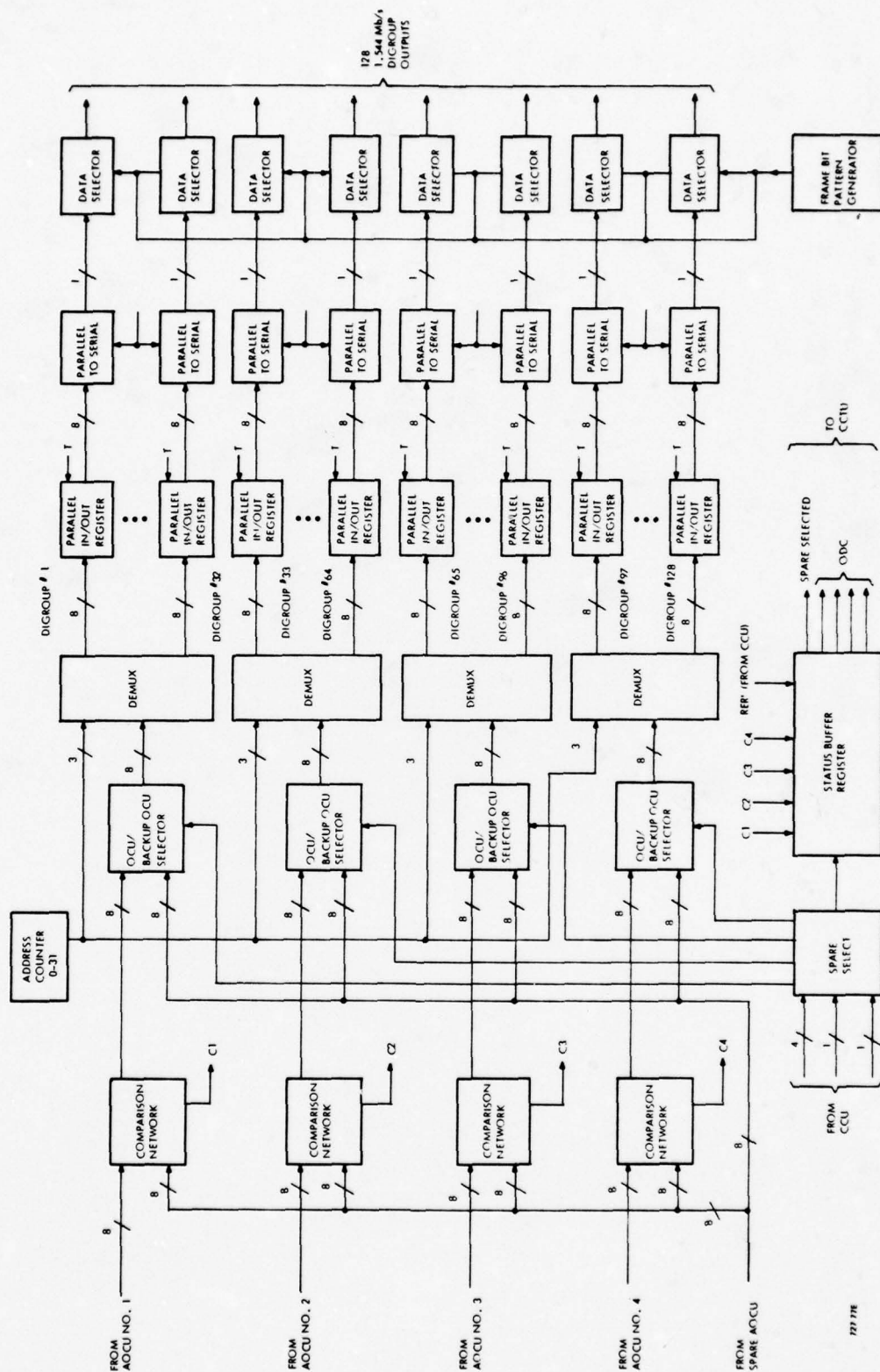


Figure 7-13. OFU Block Diagram

#### 7.2.2.1.4 Output Framing Unit (OFU)

7.2.2.1.4.1 OFU Hardware Description and Operation - The OFU performs the following functions:

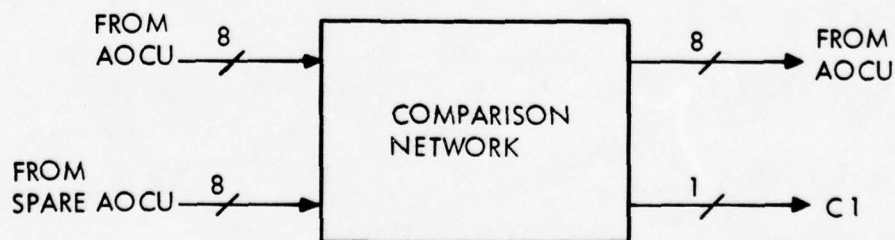
- a. Provides for bit-by-bit comparison of any AOCU data output with the spare AOCU data output for self-test purposes.
- b. Provides the capability to replace any AOCU with the spare AOCU.
- c. Converts the AOCU parallel data output to 32 serial 1.544 Mb/s T1 format digroup outputs and inserts the proper T1 frame bits.

A detailed block diagram of the OFU is provided in Figure 7-13. This diagram illustrates the OFU sized for a 128 digital group IRGA. The modularity of the OFU is discussed in Section 7.2.2.1.4.2, Partitioning of OFU Hardware Elements. The OFU consists of the following hardware elements:

- a. Comparison Network
- b. AOCU/Spare AOCU Selector
- c. Status Buffer Register
- d. Demultiplexer and Parallel In/Out Register
- e. Parallel-to-Serial Converter
- f. Frame Bit Insertion Data Selector
- g. Frame Bit Generator.

These elements are described in detail below.

7.2.2.1.4.1.1 Comparison Network - The Comparison Network is shown in Figure 7-14.



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Figure 7-14. Comparison Network



Figure 7-15 illustrates a portion of the AOCU and Spare AOCU 6.176 MHz parallel output bit streams. Each 162 ns, the Comparison Network performs the following comparisons:

$B_0$  with  $B_0'$

$B_1$  with  $B_1'$

$B_2$  with  $B_2'$

$B_3$  with  $B_3'$

$B_4$  with  $B_4'$

$B_5$  with  $B_5'$

$B_6$  with  $B_6'$

$B_7$  with  $B_7'$

If any one of these comparisons results in  $B_n \neq B_n'$ , then the Comparison Network sets its C output to a logic "1" which sets a bit in the Status Buffer Register to a logic "1".

7.2.2.1.4.1.2 AOCU/Spare AOCU Selector - This hardware element has two inputs:

- a. AOCU Output
- b. Spare AOCU Output.

Under the control of the CCU, this hardware element will select either one of the inputs and pass it to the Demultiplexer.

7.2.2.1.4.1.3 Status Buffer Register - This hardware element stores the Comparison Network status outputs. In addition, it stores a bit which indicates that the Spare AOCU output has been selected in place of one of the AOCU outputs.

7.2.2.1.4.1.4 Demultiplexer - The input to the Demultiplexer is shown in Figure 7-16. The hardware demultiplexes this input into 32 separate parallel data streams (parallel format digroups). The Demultiplexer includes a parallel in/parallel out register to time align the 32 parallel digroups after they have been demultiplexed.

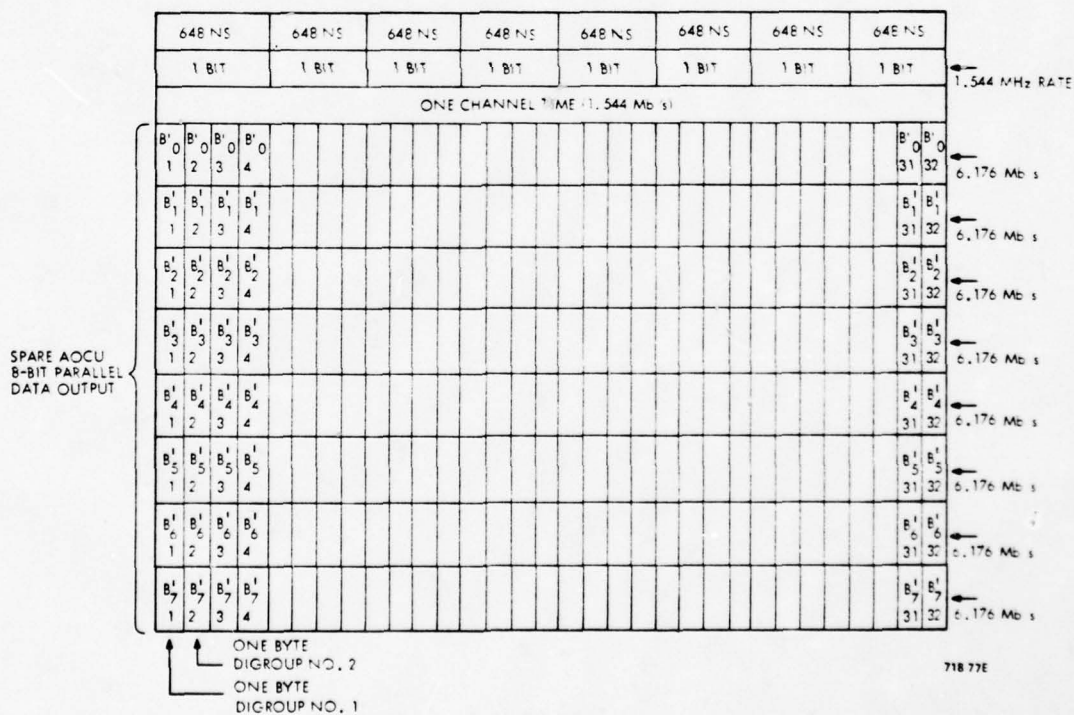
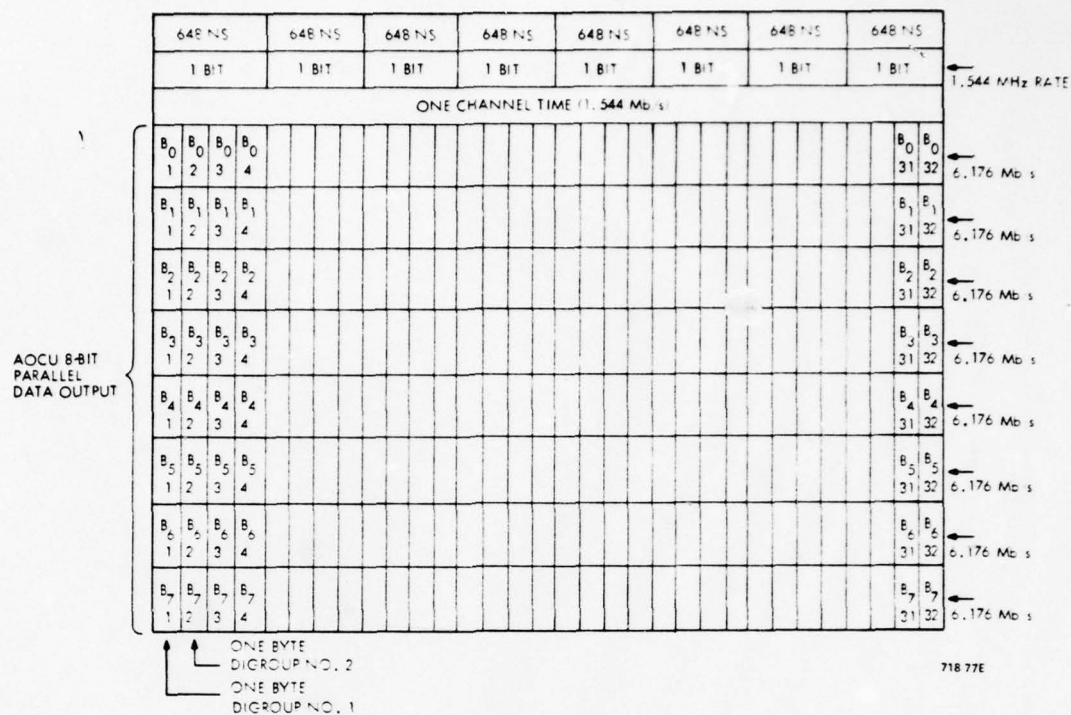
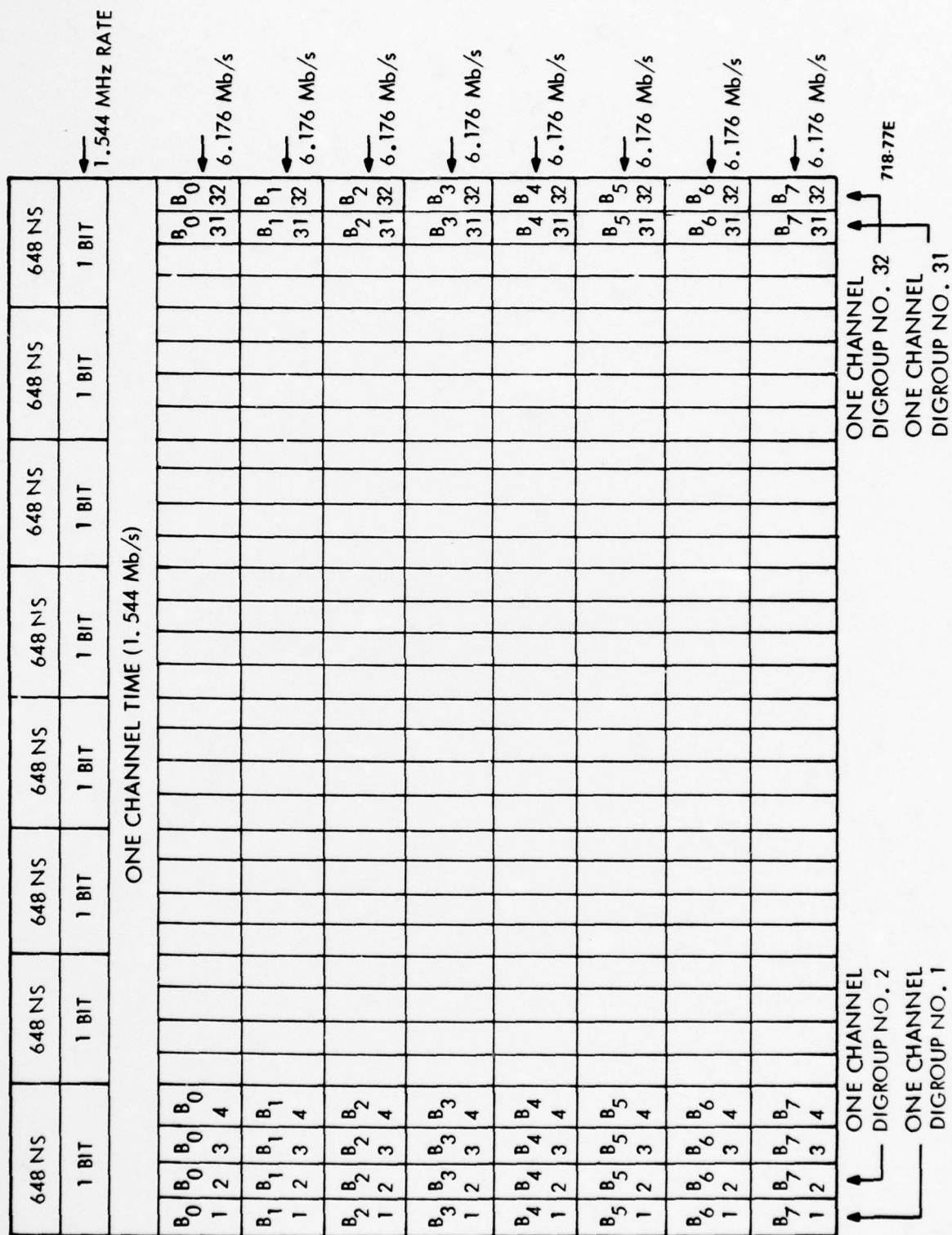


Figure 7-15. AOCU/Spares AOCU Bit Streams





7.2.2.1.4.1.5 Parallel to Serial Converter - Each demultiplexed 8-bit parallel digroup output from the Demultiplexer is passed through a parallel-to-serial converter. The output is a serial 1.544 Mb/s bit stream.

7.2.2.1.4.1.6 Frame Bit Insertion Data Selector - During one T1 frame (193 bits), the parallel-to-serial converter will provide the 192 channel bits. The Frame Bit Insertion Data Selector will insert the 193rd bit (T1 frame bit) into the data stream. The output of this hardware element is a T1 format digroup.

7.2.2.1.4.1.7 Frame Bit Generator - This hardware element provides the T1 frame bit pattern to the Frame Bit Insertion Data Selector.

7.2.2.1.4.2 Partitioning of OFU Hardware Functions - The OFU is designed to be modularly expandable to service up to a maximum of 192 digroups. To accomplish this, the OFU hardware is partitioned onto three printed circuit card types as follows:

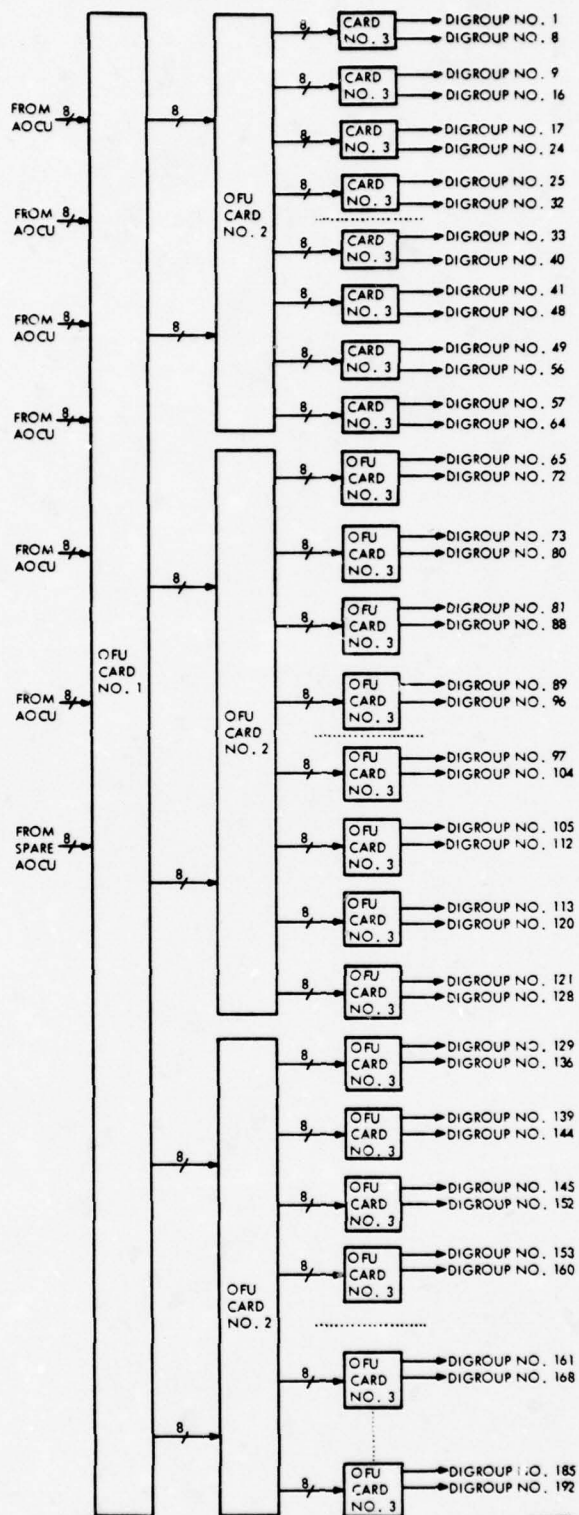
- a. OFU Card No. 1 (services up to 192 digital groups)
- b. OFU Card No. 2 (services up to 64 digital groups)
- c. OFU Card No. 3 (services up to 8 digital groups).

Table 7-15 indicates the number of each card type versus the basic DCE IRGA size in increments of 32 digroups. Figure 7-17 illustrates the interconnection of OFU cards for the maximum size IRGA (192 digroups).

Referring to Figure 7-13, the OFU hardware elements are partitioned among the four OFU card types as follows:

TABLE 7-15. OFU CARD REQUIREMENTS VERSUS IRGA SIZE

IRGA SIZE (DIGROUPS)	OFU CARD NO. 1	OFU CARD NO. 2	OFU CARD NO. 3
32	1	1	4
64	1	1	8
96	1	2	12
128	1	2	16
160	1	3	20
192	1	3	24



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Figure 7-17. Interconnection of OFU Cards

- a. OFU Card No. 1 - OFU Card No. 1 contains the following hardware elements:
  - 1. Six Comparison Networks
  - 2. Six AOCU/Spare AOCU Selectors
  - 3. Status Buffer Register.
- b. OFU Card No. 2 - OFU Card No. 2 contains part of two demultiplexers.
- c. OFU Card No. 3 - OFU Card No. 3 contains the following hardware elements:
  - 1. Eight Demultiplexers
  - 2. Eight Parallel-to-Serial Converters
  - 3. Eight Frame Bit Insertion Data Selectors
  - 4. Frame Bit Generator.



#### 7.2.2.2 Interface and Reassignment Group B (IRGB)

A block diagram of the IRGB is shown in Figure 7-18. A detailed description of the overall operation and functions performed by the IRGB is contained in Section 6.2.1.2.

The IRGB is comprised of five basic functional hardware units:

- a. Input Framing and Conversion Unit (IFCU)
- b. B Data Memory Unit (BDMU)
- c. B Output Control Unit (BOCU)
- d. Output Framing and Conversion Unit (OFCU)
- e. Subchannel Reassignment Subgroup (SRS).

The IFCU and OFCU provide the basic function of interfacing the TRI-TAC and AUTOSEVOCOM II digroups with the DCE. The BDMUs and BOCUs provide the basic channel reassignment function under the control of the Central Control Unit (in the Common Equipment Group).

The IRGB is modularly expandable in increments of 5 digroups up to the maximum capability shown in Table 7-16. Table 7-17 provides the IRBG printed circuit card requirements for each IRGB hardware unit versus the IRGB digroup capacity.

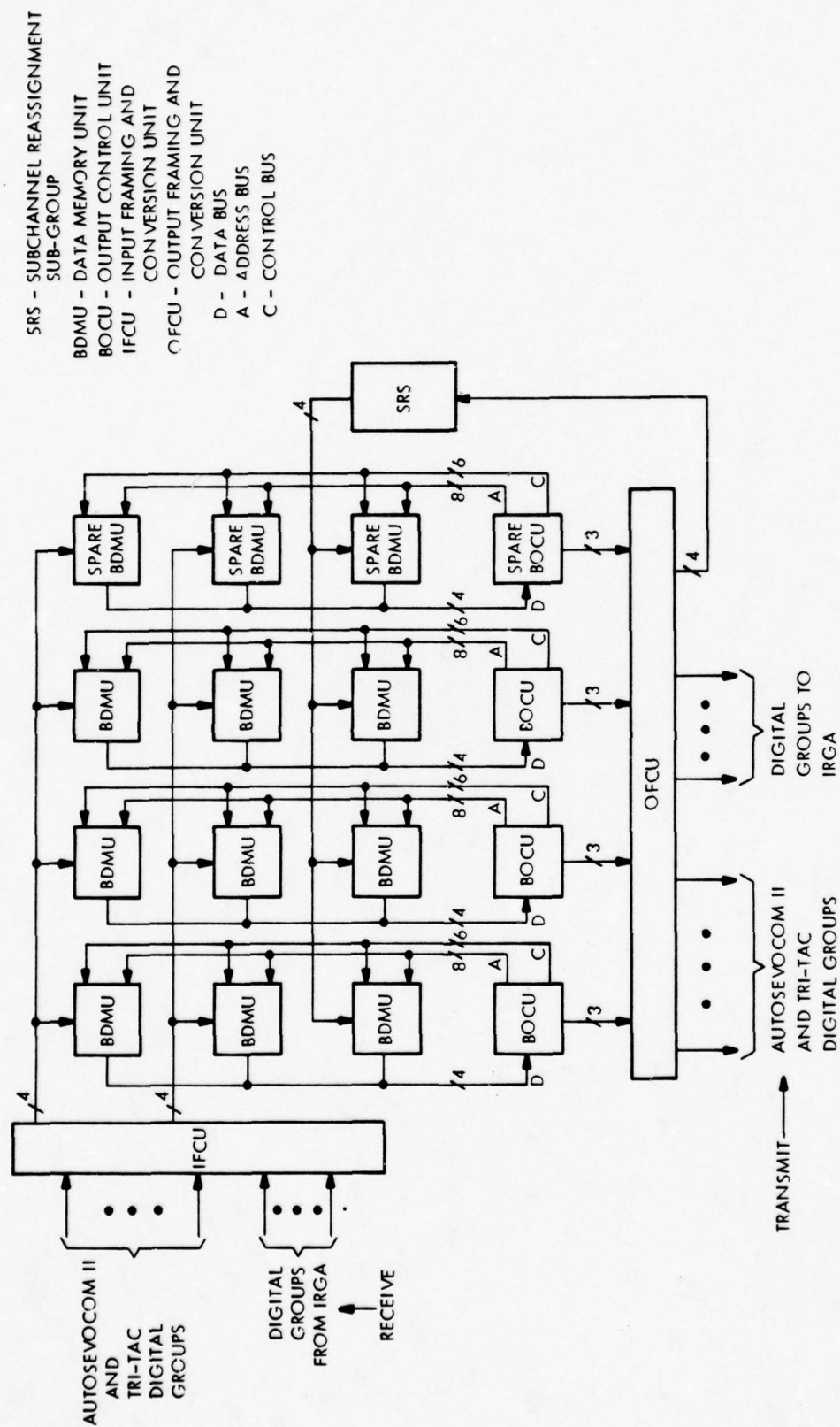
TABLE 7-16. IRGB MAXIMUM CAPABILITIES

IRGB CAPABILITY	AUTOSEVOCOM II	TRI-TAC
Number of Digital Groups	40	10
Maximum Value of "N"	95	47
Maximum Number of Channels	960	96
Maximum Number of Subchannels	960	96
Maximum Number of N = 95/47 Groups	10	2

Figure 7-19 illustrates in detail the IRGB size for a maximum of three 1.536-Mb/s terminating digroups or up to 15 lower rate terminating digroups. The number and types of printed circuit cards is shown for each unit of the IRGB. Also shown are the signal and control lines between the units. Figure 7-20 is a hardware family tree of the IRGB.

##### 7.2.2.2.1 Input Framing and Conversion Unit (IFCU)

7.2.2.2.1.1 IFCU Operation and Hardware Description - The IFCU can accept a maximum of 50 input digroups (TRI-TAC format) which terminate at the DCE. It combines these digroups into a maximum of 12 1.544-Mb/s T1 format digroups. The IFCU can accept a maximum of



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NOTE : CONFIGURED FOR A MAXIMUM OF 3 1.536 Mb/s DIGITAL GROUPS TERMINATING AT THE DCE

Figure 7-18. Interface and Reassignment Group B

TABLE 7-17. DCE IRGB CARD REQUIREMENTS VERSUS  
NUMBER OF IFCU DIGROUP OUTPUTS

NUMBER OF IFCU OUTPUTS	NUMBER OF IFCU CARDS	NUMBER <sup>1</sup> OF BDMU CARDS	NUMBER <sup>1</sup> OF BOCU CARDS	NUMBER OF OFCU CARDS	NUMBER <sup>1</sup> OF SRS CARDS	TOTAL NUMBER OF IRGB CARDS
6 NOTE 2	11	4	4	6	4	29
12 NOTE 3	17	6	6	9	4	42
18 NOTE 4	27	8	8	12	4	59
24 NOTE 5	33	10	10	15	4	72

NOTE 1. INCLUDING SPARES.

NOTE 2. TOTAL OF 15 INPUT TRUNK GROUPS TO IFCU.

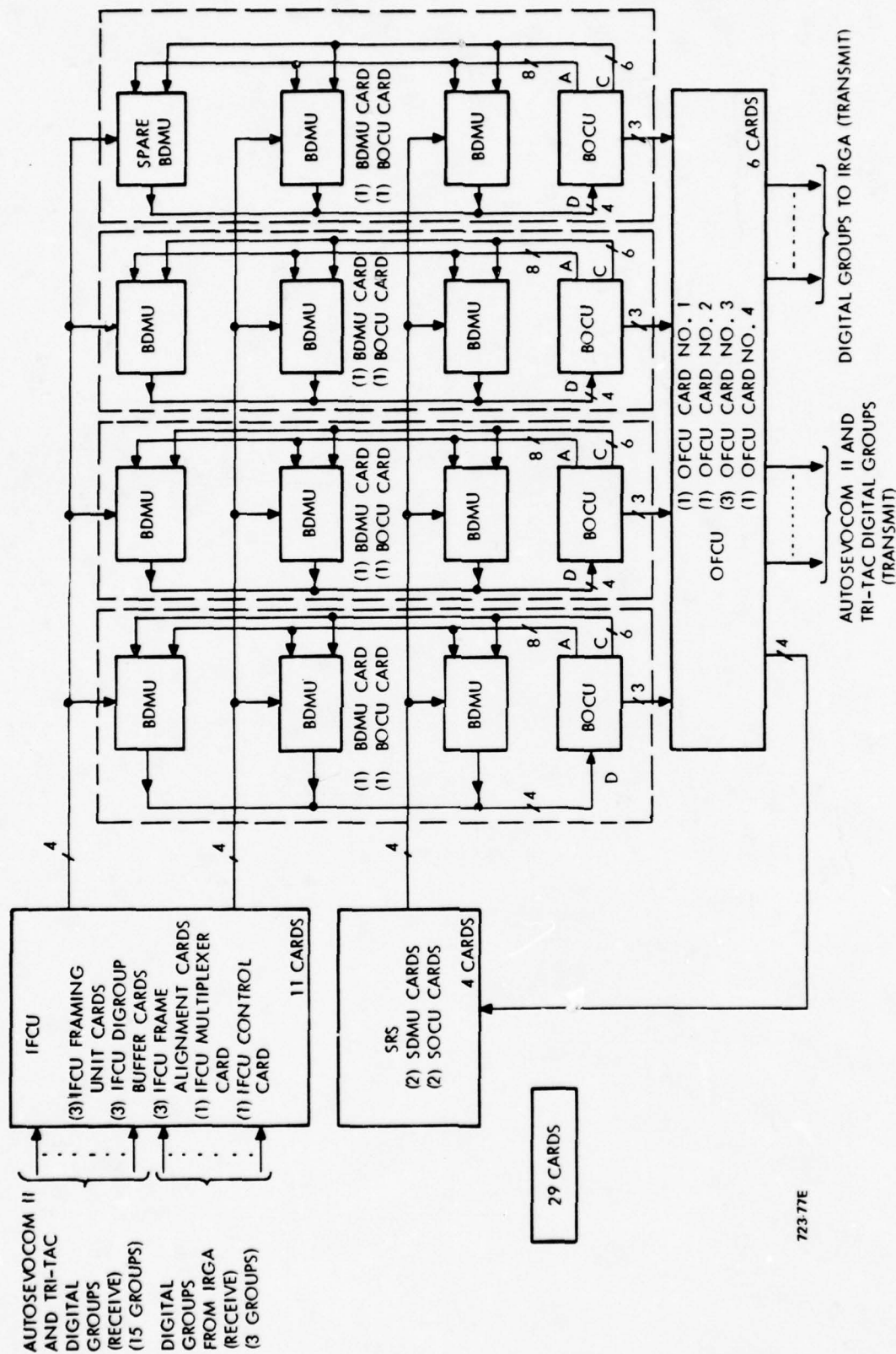
NOTE 3. TOTAL OF 25 INPUT TRUNK GROUPS TO IFCU.

NOTE 4. TOTAL OF 40 INPUT TRUNK GROUPS TO IFCU.

NOTE 5. TOTAL OF 50 INPUT TRUNK GROUPS TO IFCU.

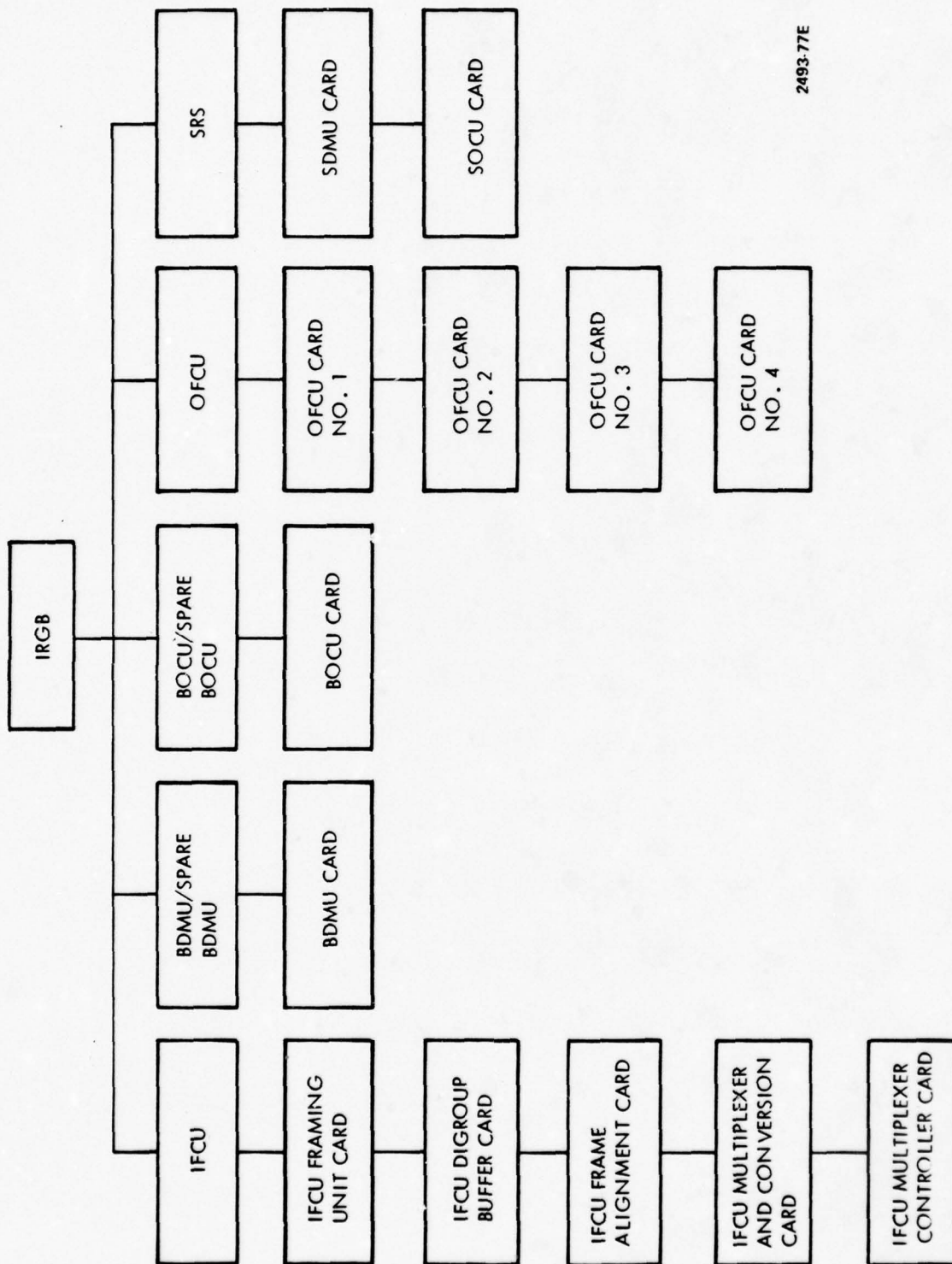
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Figure 7-19. DCE IRGB Configured for a Maximum of 3 1.536-Mb/s Trunk Group Inputs to IFCU



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Figure 7-20. IRGB Hardware Family Tree

12 1.536-Mb/s input digroups with no other digroup inputs. Each of these 1.536 Mb/s TRI-TAC digroups will occupy one of the 1.544 Mb/s T1 format digroups output by the IFCU. Table 7-18 provides the details of the TRI-TAC format digroups which can be accepted by the IFCU. The IFCU is modular in both the number of input digroups it can accept and in the number of combined 1.544 Mb/s T1 format digroups it produces. The IFCU output is modular in increments of 3 1.544-Mb/s T1 digroups (containing combined input digroups). The IFCU also accepts up to 12 1.544-Mb/s digroups from the IRGA OFU.

A detailed block diagram of the IFCU is provided in Figure 7-21.

The IFCU consists of the following hardware elements:

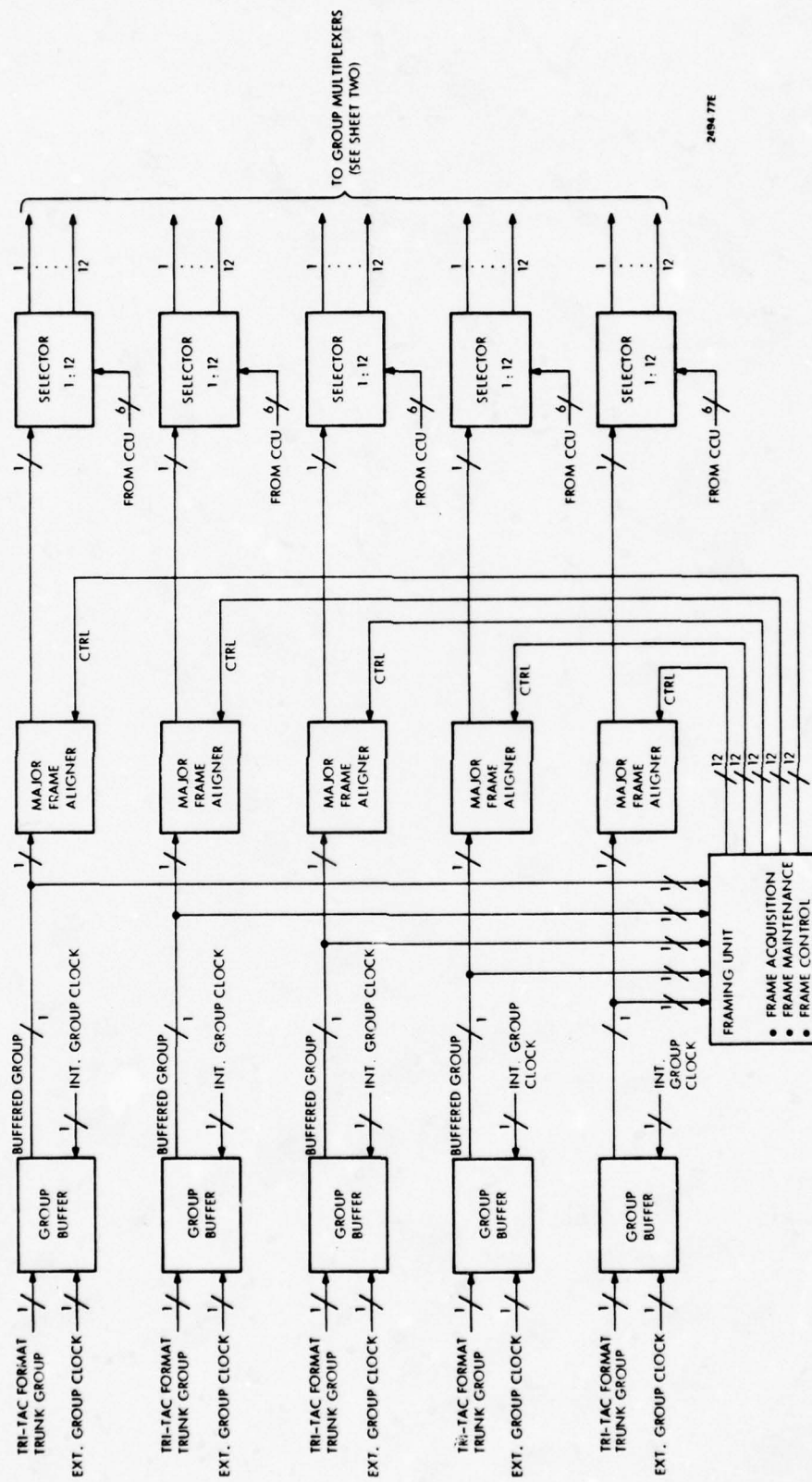
- a. Digital Group Buffer - The IFCU will provide a Digital Group Buffer for each Tactical or AUTOSEVOCOM II digital group terminating at the DCE IRGB. These buffers compensate for transmission variations and timing differences between the DCE Master Timing Unit and the recovered group clock for each digital group. In Section 6.4.2, it was shown that a 206-bit buffer is required. The Digital Group Buffer is a 256-bit FIFO elastic buffer.
- b. Major Frame Alignment Buffer - A buffer is provided for each terminating Tactical or AUTOSEVOCOM II digital group. This buffer has a capacity of 8 TRI-TAC major frames of a 96 channel digital group. Under the control of the Framing Unit, these buffers master frame (8 TRI-TAC minor frames) align all the input Tactical and AUTOSEVOCOM II digital groups to an interval DCE master frame reference.
- c. Framing Unit - The Framing Unit services up to five terminating TRI-TAC format digital groups. It performs frame acquisition, frame maintenance, detection and reporting (to the CCU) of loss-of-frame and control of up to five Master Frame Alignment Buffers. In addition, it controls the transmit frame pattern generators in the OFCU for each of the 5 terminating digital groups.
- d. Group Multiplexer and Combiner Selector - The hardware element is provided to route each digroup to one of twelve Group Multiplexer and Combiners. The selection is made under CCU control.



TABLE 7-18. TRI-TAC FORMAT DIGROUPS ACCEPTED BY THE IFCU

TOTAL CHANNELS (INCLUDES PRIMARY OVERHEAD CHANNEL)	MAXIMUM AVAILABLE TRAFFIC CHANNELS	DIGROUP BIT RATE (AT VDR OF 16 KB/S) IN KB/S	DIGROUP BIT RATE (AT VDR OF 32 KB/S) IN KB/S
8	7	128	256
9	8	144	288
16	15	256	512
18	17	288	576
32	31	512	1024
36	35	576	1152
48	47	NOTE 1	1536
64	63	1024	--
72	71	1152	--
96	95	1536	--

NOTE: 1 No TRI-TAC/AUTOSEVOCOM group exists.



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Figure 7-21. Input Framing and Conversion Unit Block Diagram (Sheet 1 of 2)

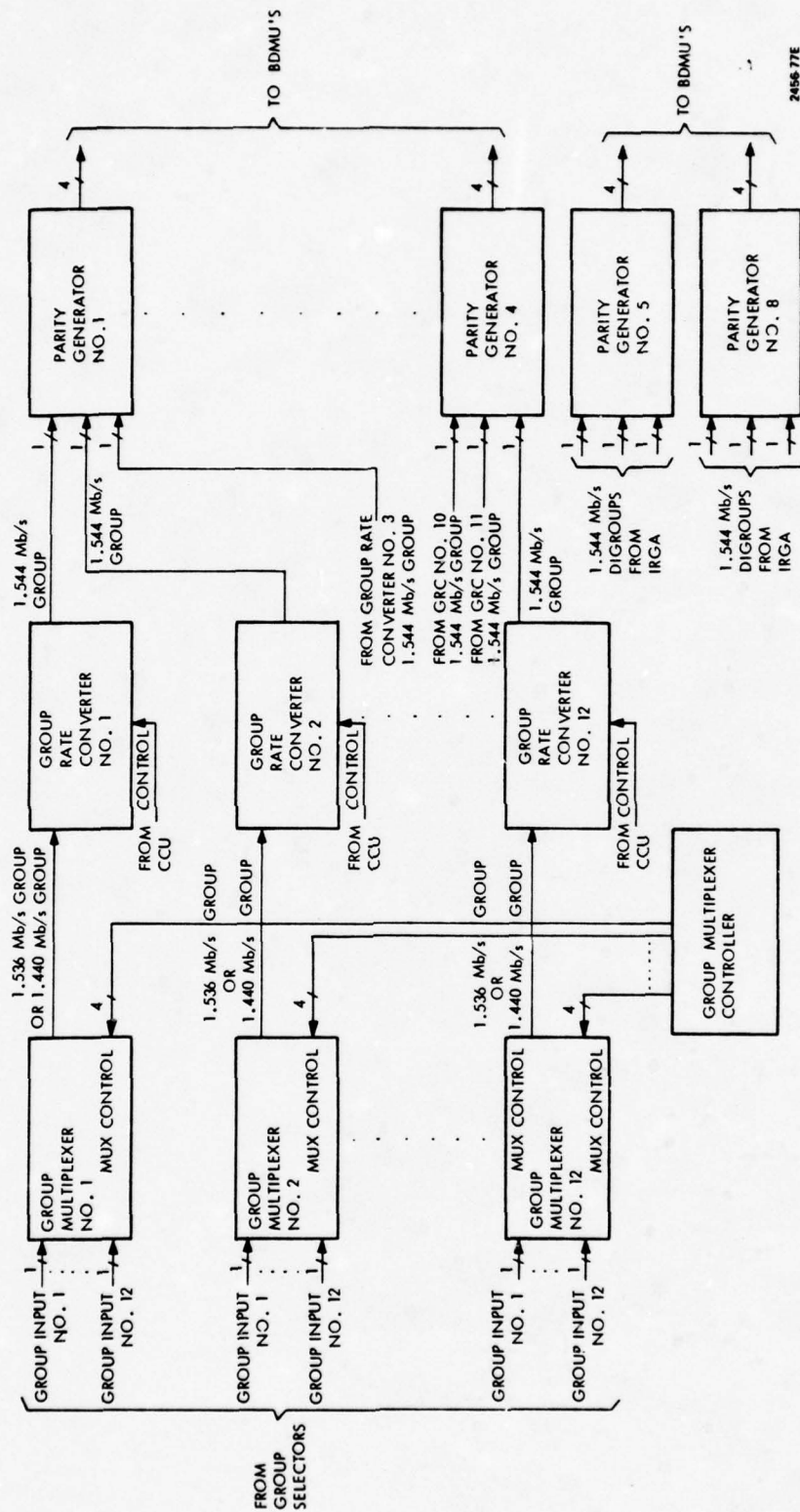


Figure 7-21. Input Framing and Conversion Unit Block Diagram (Sheet 2 of 2)



- e. Group Multiplexer and Combiner - The Group Multiplexer and Combiner is provided to combine TRI-TAC format input digroups into a 1.544 Mb/s T1 format digroup. Referring to Table 7-18, the input digroup bit rates accepted by the IFCU can be divided in two groups (except 1.536 Mb/s) as follows:

1.  $8,000 \times 2^n$  b/s Rates - These rates are an even multiple of 8 kb/s. Table 7-19 illustrates this concept.

TABLE 7-19.  $8,000 \times 2^n$  B/S RATES

n	RATE (KB/S)	VDR (KB/S)
4	128	16
5	256	16, 32
6	512	16, 32
7	1024	16, 32

2.  $9,000 \times 2^m$  b/s Rates - These rates are an even multiple of 9 kb/s. Table 7-20 illustrates this concept.

TABLE 7-20.  $9,000 \times 2^m$  B/S RATES

m	RATE (KB/S)	VDR (KB/S)
4	144	16, 32
5	288	16, 32
6	576	16, 32
7	1152	16, 32

3. 1,536 Mb/s Rate - This rate does not fall into either of the two preceding groups.

There are two Group Multiplexer and Combiner Types. One type accepts all the  $8,000 \times 2^n$  digroup rates plus the 1.536 Mb/s digroup rate and produces a 1.536 Mb/s output digroup. The other type accepts all the  $9,000 \times 2^m$  digroup rates and produces a 1.440 Mb/s output digroup. Table 7-21 illustrates the various input options for the  $8,000 \times 2^n$  Group Multiplexer and Combiner.

TABLE 7-21. VARIOUS DIGROUP INPUT OPTIONS FOR THE  $8,000 \times 2^n$  GROUP MULTIPLEXER AND COMBINER

128 KB/S	256 KB/S	512 KB/S	1024 KB/S	1536 KB/S	CASE NO.
0	0	1	1	0	1
0	2	0	1	0	2
2	1	0	1	0	3
4	0	0	1	0	4
0	0	3	0	0	5
0	2	2	0	0	6
2	1	2	0	0	7
4	0	2	0	0	8
0	4	1	0	0	9
2	3	1	0	0	10
4	2	1	0	0	11
6	1	1	0	0	12
0	6	0	0	0	13
2	5	0	0	0	14
4	4	0	0	0	15
6	3	0	0	0	16
8	2	0	0	0	17
10	1	0	0	0	18
12	0	0	0	0	19
0	0	0	0	1	20

Table 7-22 illustrates the various input options for the 9,000 x 2<sup>m</sup> Group Multiplexer and Combiner. The two types utilize the same hardware circuitry but use different timing and control signals.

TABLE 7-22. VARIOUS DIGROUP INPUT OPTIONS FOR THE 9,000 x 2<sup>m</sup> GROUP MULTIPLEXER & COMBINER

144 KB/S	288 KB/S	576 KB/S	1152 KB/S	CASE NO.
0	1	0	1	1
2	0	0	1	2
0	1	2	0	3
0	3	1	0	4
2	2	1	0	5
4	1	1	0	6
6	0	1	0	7
0	5	0	0	8
2	4	0	0	9
4	3	0	0	10
6	2	0	0	11
8	1	0	0	12
10	0	0	0	13

- f. A Group Rate Converter is provided to bring the output of the Group Multiplexer and Combiner from 1.440 Mb/s or 1.536 Mb/s up to 1.544 Mb/s.
- g. A Group Multiplexer Controller controls the order in which input digroups are combined. This hardware element controls up to 12 Group Multiplexers and is under CCU control.



- h. A Parity Generator is provided for three 1.544-Mb/s digroup outputs from three Group Rate Converters. The output of the Parity Generator is a parallel 4-bit data stream at 1.544 Mb/s. The fourth bit is a parity bit. This data stream is routed to the B Data Memory Units.

7.2.2.2.1.2 Partitioning of IFCU Hardware Elements - The IFCU hardware is partitioned onto five printed circuit card types as follows:

- |   |   |                                  |
|---|---|----------------------------------|
| a. IFCU Framing Unit Card               | } | Basic IFCU<br>Modular<br>Element |
| b. Digroup Buffer Card                  |   |                                  |
| c. IFCU Frame Alignment Card            |   |                                  |
| d. IFCU Multiplexer and Conversion Card |   |                                  |
| e. IFCU Multiplexer Control Card.       |   |                                  |

With the exception of the IFCU Multiplexer and Conversion Card and the IFCU Multiplexer Controller Card, each IFCU card is designed to service up to five TRI-TAC formatted digital groups terminating at the DCE IRGB. The IFCU Multiplexer and Conversion Card provides a capacity of multiplexing terminating TRI-TAC format digital groups into six 1.544-Mb/s output groups. In addition, this card accepts up to six 1.544-Mb/s digital groups from the IRGA OFU. These six groups are grouped three together and each group of 3 is passed through Parity Generator. Therefore, the IFCU Multiplexer and Conversion Card provides up to 12 1.544-Mb/s digital group outputs (six groups of combined TRI-TAC format digital groups plus six 1.544-Mb/s groups from the IRGA OFU). The IFCU Multiplexer Controller Card services up to 50 TRI-TAC formatted digital groups which terminate at the DCE IRGB. The basic IFCU modular element for five TRI-TAC format input digital groups consists of three printed circuit cards. Table 7-23 indicates the number of each IFCU card type versus the IFCU size. The IFCU size is determined by two factors, the number of 1.544 Mb/s output digital groups it provides and the number of TRI-TAC formatted digital groups which terminate at the IFCU.

Referring to Figure 7-21, the IFCU hardware functions are partitioned among the five IFCU card types as follows:

- a. IFCU Framing Unit Card - This card contains the Framing Unit.
- b. IFCU Digroup Buffer Card - This card contains five Group Buffers.
- c. IFCU Frame Alignment Card - This card contains five Master Frame Alignment Buffers (8 TRI-TAC minor frames), and five Group Multiplexer and Combiner Selectors.

TABLE 7-23. IFCU CARD REQUIREMENTS VERSUS IFCU SIZE

NUMBER OF 1.544 MB/S DIGITAL GROUP OUTPUTS FROM THE IFCU	NUMBER OF IFCU FRAMING UNIT CARDS	NUMBER OF IFCU DIGROUP BUFFER CARDS	NUMBER OF IFCU FRAME ALIGNMENT CARDS	NUMBER OF IFCU MULTIPLEXER AND CONVERSION CARDS	NUMBER OF IFCU MULTIPLEXER CONTROLLER CARDS
6 ①	3	3	3	1	1
12 ②	5	5	5	1	1
18 ③	8	8	8	2	1
24 ④	10	10	10	2	1

- NOTES:
- ① Total of 15 TRI-TAC format input digital groups to the IFCU.
  - ② Total of 25 TRI-TAC format input digital groups to the IFCU.
  - ③ Total of 40 TRI-TAC format input digital groups to the IFCU.
  - ④ Total of 50 TRI-TAC format input digital groups to the IFCU.

- d. IFCU Group Multiplexer and Conversion Card - This card contains six Group Multiplexer and Combiners, six Group Rate Converters, and four Parity Generators.
- e. IFCU Multiplexer Controller Card - This card contains the Group Multiplexer Controller hardware.

7.2.2.2.2 IRGB Time Division Memory Matrix - The IRGB Time Division Memory Matrix (TDMM) is made up of B Data Memories. The number of B Data Memories required depends on the size of the IRGB. Figure 7-21A illustrates the IRGB TDMM for each size IRGB in increments of six 1.544-Mb/s digital group outputs from the IFCU. The matrix is modular in increments of six digital groups up to a maximum of 24 digital groups. The TDMM also provides for an additional three 1.544-Mb/s inputs from the Subchannel Reassignment Subgroup (SRS). These inputs are always provided for regardless of the size of the IRGB. As discussed later, there are nine B Data Memories on one printed circuit card. These nine B Data Memories constitute one maximum size column of the IRGB TDMM. For each size TDMM, one column (one printed circuit card) is a spare column, while a second column is designated to support the SRS. The spare column is on hot standby and can be switched into service by the Central Control Unit to replace a column which has a failure. All B Data Memories are identical, including the spares.

The IRGB TDMM plus the B Output Control Units (BOCUs) provide the IRGB digital time division switching capability. The IRGB digital time division switching is bit organized as opposed to the IRGA where switching is byte (8-bits) organized. Data from the Data Input Bus is written into all the B Data Memories in a row and data is read out from the B Data Memories onto the Output Data Bus by the BOCUs, accomplishing the switching function.

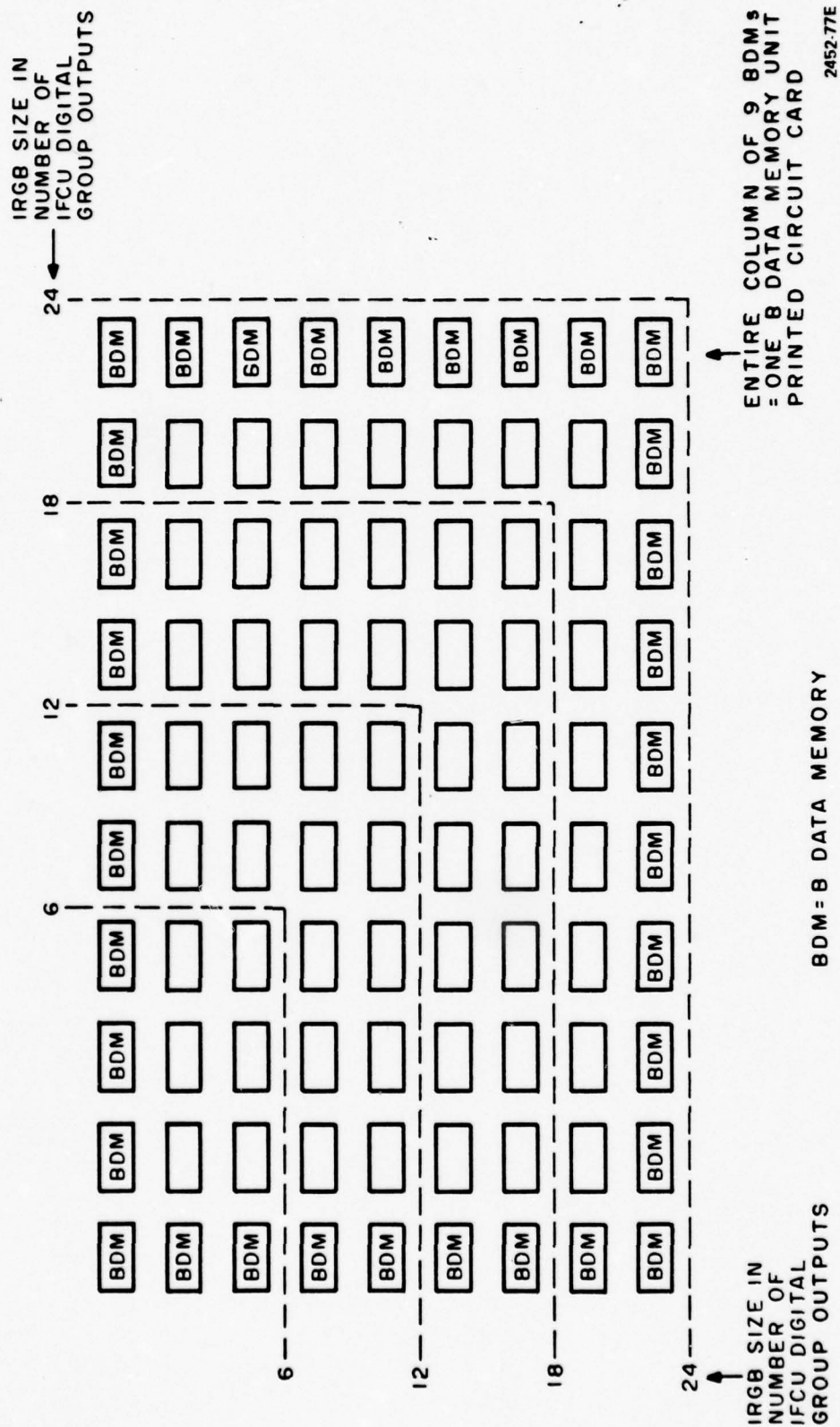
The theory of the Time Division Switching approach which is used in the IRGB is discussed in detail in Section 5.2.2. Some additional details of the operation of the IRGB TDMM are provided in Section 6.2.1.2.

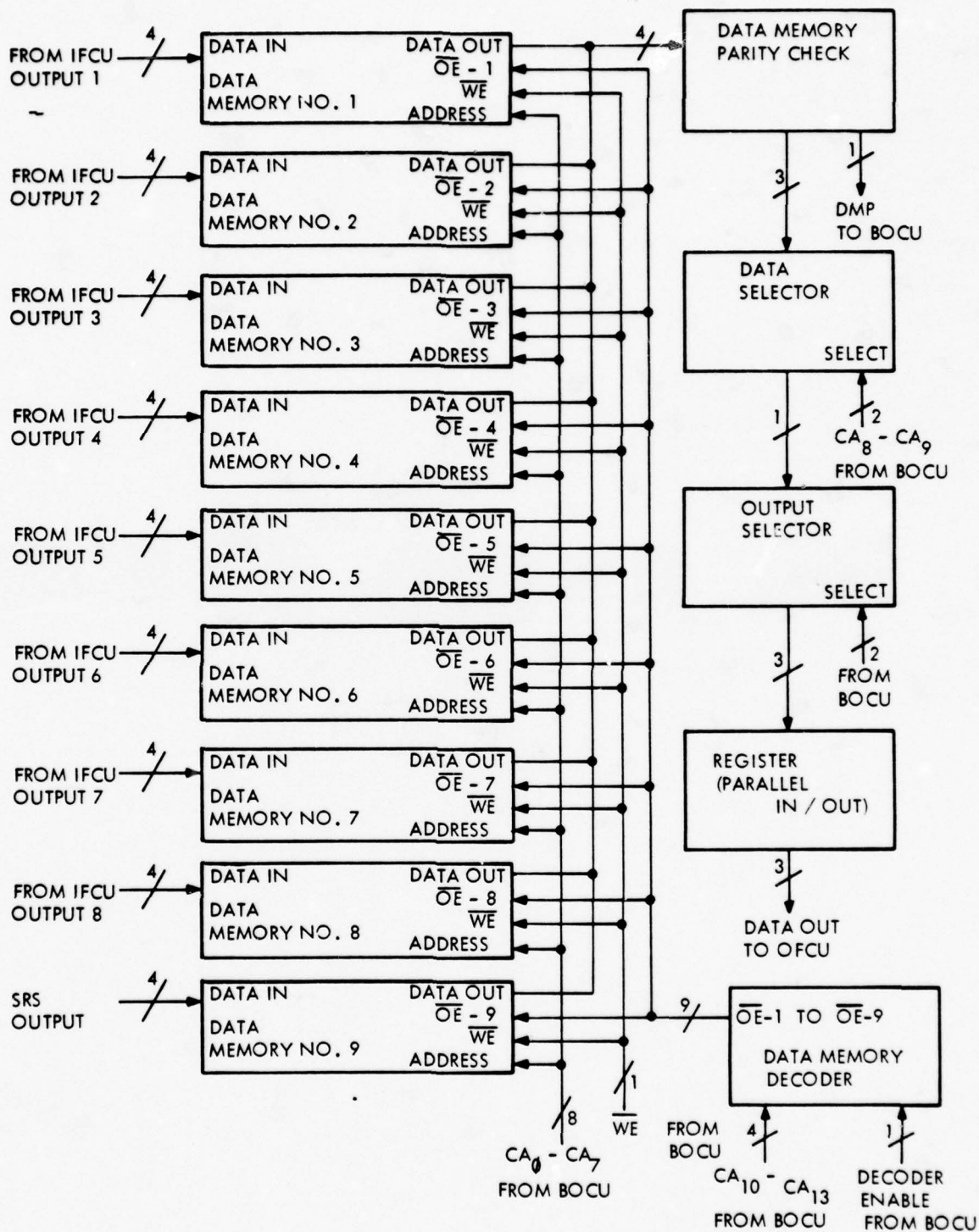
The following section provides the details of the hardware implementation of the B Data Memory which is the basic element in the IRGB TDMM.

7.2.2.2.2.1 BDMU Hardware Description - The BDMU is the heart of the IRGB Time Division Memory Matrix in that it is the element that performs the reassignment of individual TRI-TAC and AUTOSEVOCOM II channels. Each BDMU has up to 27 1.544-Mb/s digroups input to it. These digroups are in their normal serial bit stream format and the three digroups are input in parallel to the BDMU.

A detailed block diagram of the BDMU is provided in Figure 7-22. The BDMU consists of the following hardware elements (quantities are given in parentheses):







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Figure 7-22. B Data Memory Unit Block Diagram

- a. Data Memory (9)
- b. Data Memory Parity Check (1)
- c. Data Selector (1)
- d. Output Selector (1)
- e. Register (Parallel-In, Parallel-Out) (1)
- f. Data Memory Decoder (1) and Address Controller.

These hardware elements are described below.

- a. Data Memory - The Data Memory is a 192 x 4-bit Random Access Memory (RAM). This memory stores 192 T1 data bit of T1 frame for three 1.544-Mb/s digroup outputs from the IFCU or SRS. In addition, it stores a parity bit for each 3-bit word written into memory.
- b. Data Memory Parity Check - This hardware element strips off the three digroup data bits from the 4-bit words read out of the Data Memory and passes these bits in parallel to the Data Selector. It also checks the 4-bit word for odd parity and sets its DMP line to a logic "1" if odd parity is not present.
- c. Data Selector - During each read access from the Data Memory, the Data Selector selects one of the three data bits and passes it to the Output Selector. The selection is controlled by two connection address bits (CA<sub>8</sub> and CA<sub>9</sub>) from the BOCU.
- d. Output Selector - During each read access from the Data Memory, the Output Selector directs the data bit from the Data Selector to one-of-three T1 digroup output lines which go to the Register.
- e. Register - During each T1 bit time (648 ns), three read accesses are done on the Data Memory. The Register stores the three data bits (which are skewed over the 648 ns bit time) and clocks them out simultaneously which aligns them in time. The Register output is routed to the OFCU.
- f. Data Memory Decoder - The Data Memory Decoder controls which of the nine data memories is accessed during a read operation. It accepts four connection address bits (CA<sub>10</sub>, CA<sub>11</sub>, CA<sub>12</sub> and CA<sub>13</sub>) and selects one of the Data Memories. If the decoder enable signal from the BOCU is not present, none of the Data Memories is selected (this situation occurs during the write access portion of a T1 bit time).

**7.2.2.2.2.2 BDMU Hardware Operation** - Figure 7-23 illustrates the frame structure of a 1.544 Mb/s T1 digital group. Figure 7-24 illustrates a portion of the 4-bit parallel data stream (1.544 Mb/s)



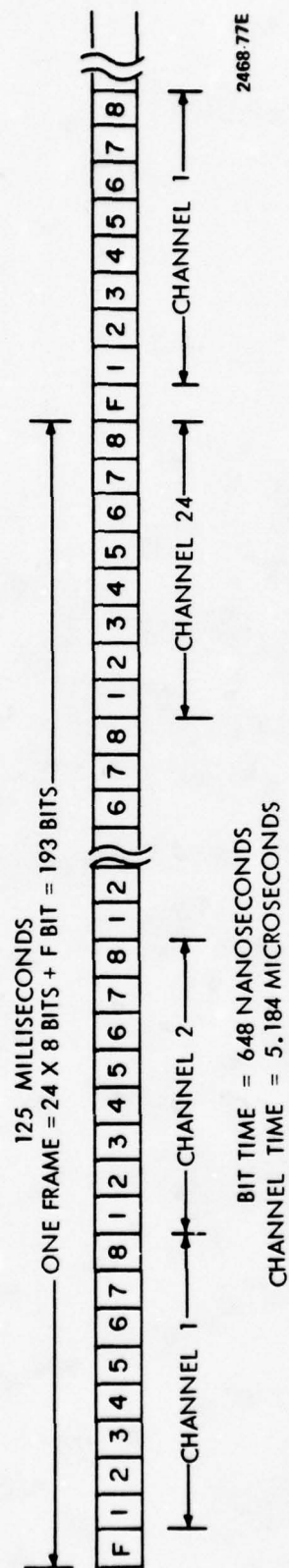


Figure 7-23. Frame Structure of a 1.544 Mb/s T1 Digital Group

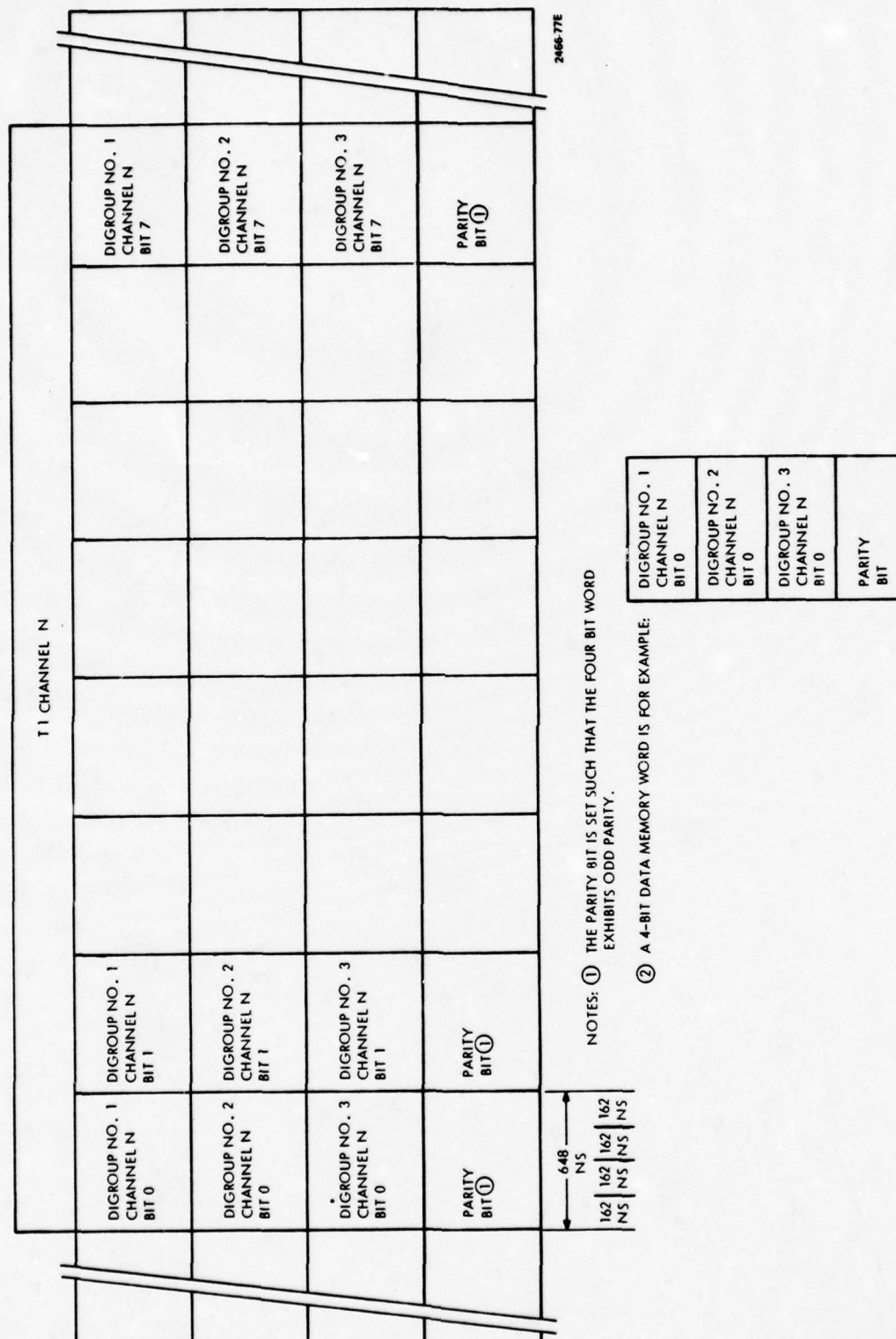


Figure 7-24. BDMU Data Memory Input from IFCU

input to the BDMU Data Memory from the IFCU. This parallel data stream contains three serial digroups plus a parity data line.

Figure 7-25 illustrates the operation of the Data Memory. Four Data Memory accesses are performed during one T1 bit time of 648 ns. Thus, every 162 ns an access is done. The first access in a T1 bit is a write of the 4-bit word which appears at the Data Memory input at the beginning of the T1 bit. This is followed by three read accesses from the Data Memory. The hardware external to the Data Memory selects one of the three bits during each read access. These bits may be selected in any sequence. The sequence of bit selection (reassignment) is controlled by the BOCU.

Figure 7-26 illustrates the content of the BDMU Register during a T1 bit time of 648 ns. During the write access, the Register is cleared. During the first read access, any one data bit from one of the 27 T1 input digroups is clocked into the Register. During the second read access, any one data bit from one of the 27 T1 input digroups is clocked into the Register. During the third read access, the Register is filled by any one data bit from one of the 27 T1 input digroups. During the third access, the 3-bit word in the Register is clocked out to the OFCU and simultaneously the Register is cleared.

#### 7.2.2.2.2.3 Partitioning of BDMU Hardware Functions - The BDMU hardware elements, namely:

- a. Data Memory (9)
- b. Data Memory Parity Check (1)
- c. Data Selector (1)
- d. Output Selector (1)
- e. Register (1)
- f. Data Memory Decoder (1)

will be packaged on one printed circuit card. Table 7-24 indicates the number of BDMU cards versus the size of the IRGB.

TABLE 7-24. BDMU CARD REQUIREMENTS VERSUS IFCU SIZE

NUMBER OF 1.544 MB/S DIGROUP OUTPUTS FROM THE IFCU	NUMBER OF BDMU CARDS ①
6	4
12	6
18	8
24	10

NOTE: ① Includes one spare BDMU card.



T1	CHANNEL		N			
DIGROUP NO. 1 CHANNEL N	BIT 0	(A <sub>1</sub> )	.....	DIGROUP NO. 1 CHANNEL N	BIT 7	(A' <sub>1</sub> )
DIGROUP NO. 2 CHANNEL N	BIT 0	(B <sub>2</sub> )	.....	DIGROUP NO. 2 CHANNEL N	BIT 7	(B' <sub>2</sub> )
DIGROUP NO. 3 CHANNEL N	BIT 0	(C <sub>3</sub> )	.....	DIGROUP NO. 3 CHANNEL N	BIT 7	(C' <sub>3</sub> )
PARITY	BIT	(P <sub>1</sub> )	.....	PARITY	BIT	(P' <sub>1</sub> )
WRITE	READ	READ	READ	WRITE	READ	READ
A <sub>1</sub> B <sub>1</sub> C <sub>1</sub> P <sub>1</sub>	A <sub>1</sub> B <sub>1</sub> C <sub>1</sub> P <sub>1</sub>	A <sub>1</sub> B <sub>1</sub> C <sub>1</sub> P <sub>1</sub>	.....	A' <sub>1</sub> B' <sub>1</sub> C' <sub>1</sub> P' <sub>1</sub>	A' <sub>1</sub> B' <sub>1</sub> C' <sub>1</sub> P' <sub>1</sub>	A' <sub>1</sub> B' <sub>1</sub> C' <sub>1</sub> P' <sub>1</sub>

Figure 7-25. BDMU Data Memory Operation

EMPTY	$A_1 \dots OR A_9 \text{ OR } B_1 \dots OR B_9 \text{ OR } C_1 \dots OR C_9$	$A_1 \dots OR A_9 \text{ OR } B_1 \dots OR B_9 \text{ OR } C_1 \dots OR C_9$	$A_1 \dots OR A_9 \text{ OR } B_1 \dots OR B_9 \text{ OR } C_1 \dots OR C_9$	EMPTY		$A_1 \dots OR A_9 \text{ OR } B_1 \dots OR B_9 \text{ OR } C_1 \dots OR C_9$	$A_1 \dots OR A_9 \text{ OR } B_1 \dots OR B_9 \text{ OR } C_1 \dots OR C_9$	$A_1 \dots OR A_9 \text{ OR } B_1 \dots OR B_9 \text{ OR } C_1 \dots OR C_9$
EMPTY	EMPTY	$A_1 \dots OR A_9 \text{ OR } B_1 \dots OR B_9 \text{ OR } C_1 \dots OR C_9$	$A_1 \dots OR A_9 \text{ OR } B_1 \dots OR B_9 \text{ OR } C_1 \dots OR C_9$	EMPTY	$A_1 \dots OR A_9 \text{ OR } B_1 \dots OR B_9 \text{ OR } C_1 \dots OR C_9$	EMPTY	EMPTY	EMPTY
EMPTY	EMPTY	EMPTY	$A_1 \dots OR A_9 \text{ OR } B_1 \dots OR B_9 \text{ OR } C_1 \dots OR C_9$	EMPTY	$A_1 \dots OR A_9 \text{ OR } B_1 \dots OR B_9 \text{ OR } C_1 \dots OR C_9$	EMPTY	EMPTY	EMPTY

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Figure 7-26. BDMU Register Content

#### 7.2.2.2.3 B Output Control Unit (BOCU)

7.2.2.2.3.1 BOCU Hardware Description and Operation - The BOCU controls the BDMUs to perform channel reassignment. The BOCU interfaces directly with the Central Control Unit (CCU) in the Common Equipment Group (CEG).

A detailed block diagram of the BOCU is provided in Figure 7-27. The BOCU consists of the following hardware elements;

- a. Command Parity Check Function
- b. Address Memory
- c. Output Controller Function
- d. Address Memory Parity Check Function
- e. Data Memory Parity Check Encoder Function
- f. Connection Address Register
- g. Parity Status Register.

These hardware elements which are described in detail below are quite similar to their corresponding hardware elements in the AOCU.

- a. Command Parity Check Function - The CCU controls the BOCU via a 31-bit parallel command interface. CCU commands are received by the Command Parity Check Function. Figure 7-28 illustrates the various fields in the CCU command. The Command Parity Check Function checks the parity of the 31-bit command. If the 31-bits do not display odd parity, then the CDMP output is set to a logic "1" and the CDMP status bit is set to a "1" in the Parity Status Register. Also, the command is inhibited from acting on other BOCU hardware by disabling the RCA' and WCA' outputs. The Command Parity Check Function also strips the CA and LOC fields off the command and sends these to the Address Memory and the Output Controller Function, respectively.
- b. Address Memory - The address Memory is a 576 x 15-bit RAM. It stores 576 connection addresses (CA<sub>0</sub>-CA<sub>14</sub>). The connection address determines which of the nine B Data Memories on a BDMU a BOCU will read from and which of the three channel bits read out will be passed to the BDMU Register. The channel reassignment function of the IRGB resides in the sequence of connection addresses stored in the Address Memory. The connection addresses are written into the Address Memory by the CCU; one connection address is written during each T1 frame bit. During a T1 data bit time, there are three read accesses performed on the Address Memory. This is illustrated in Figure 7-29. Under the control of the CCU, one connection address may be read from or written into the Address Memory during the T1 frame bit time.



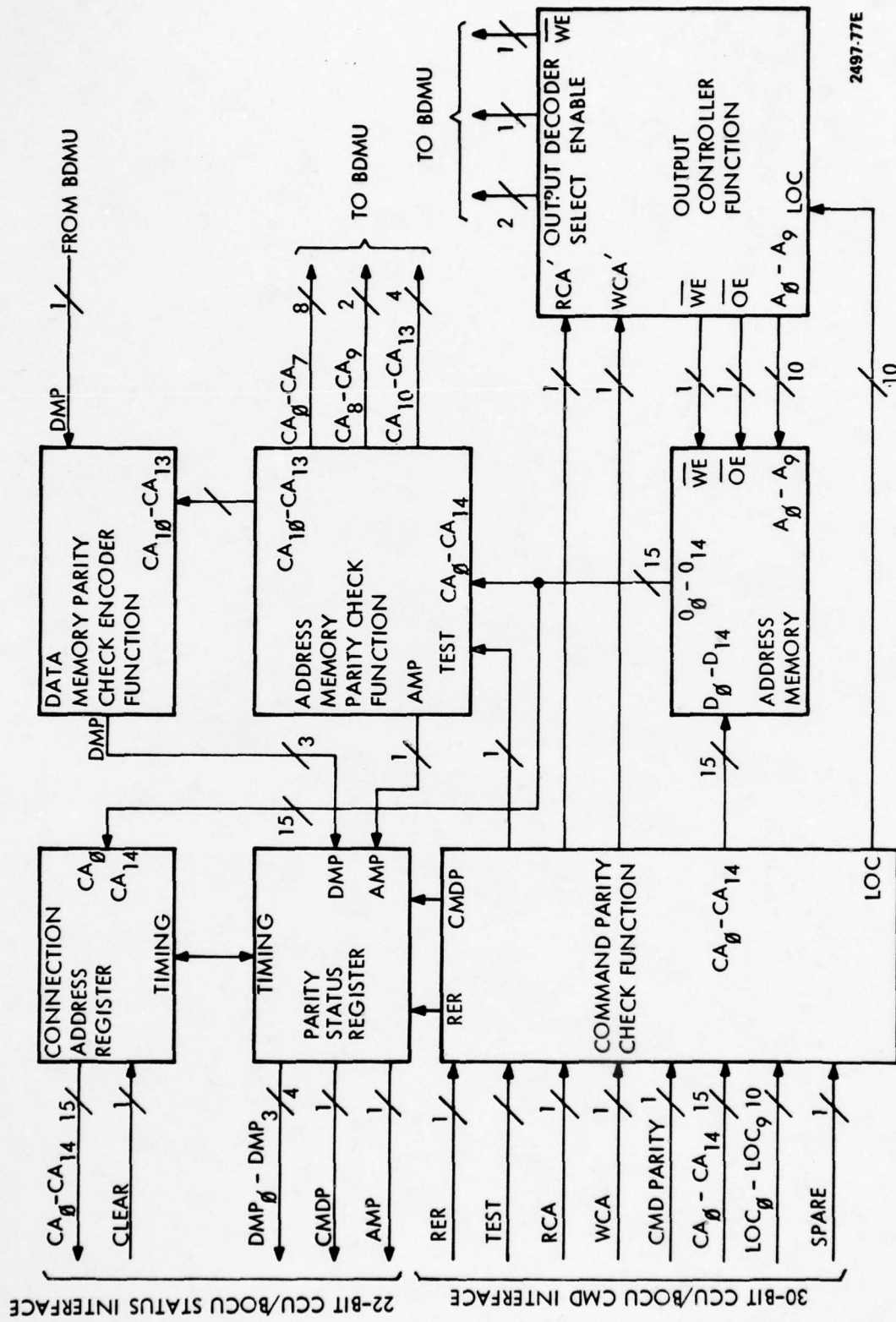
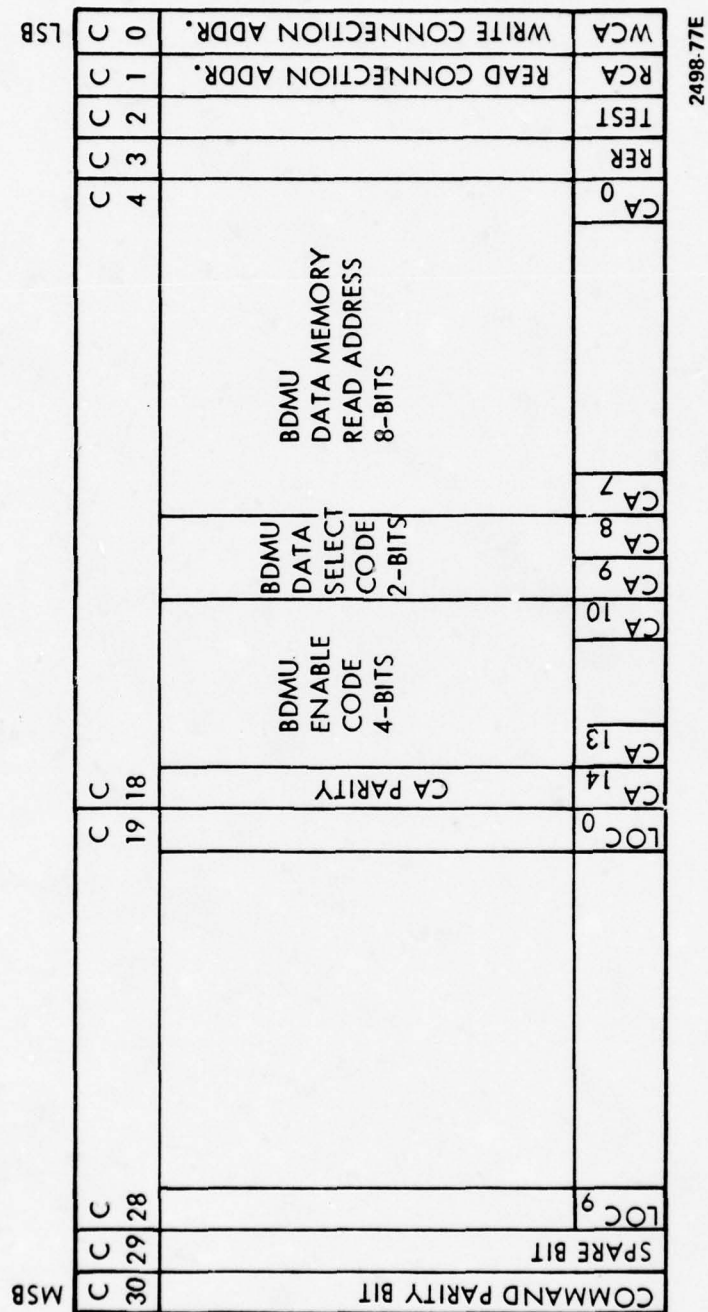


Figure 7-27. B Output Control Unit Block Diagram



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Figure 7-28. CCU Command Format for BOCU Control

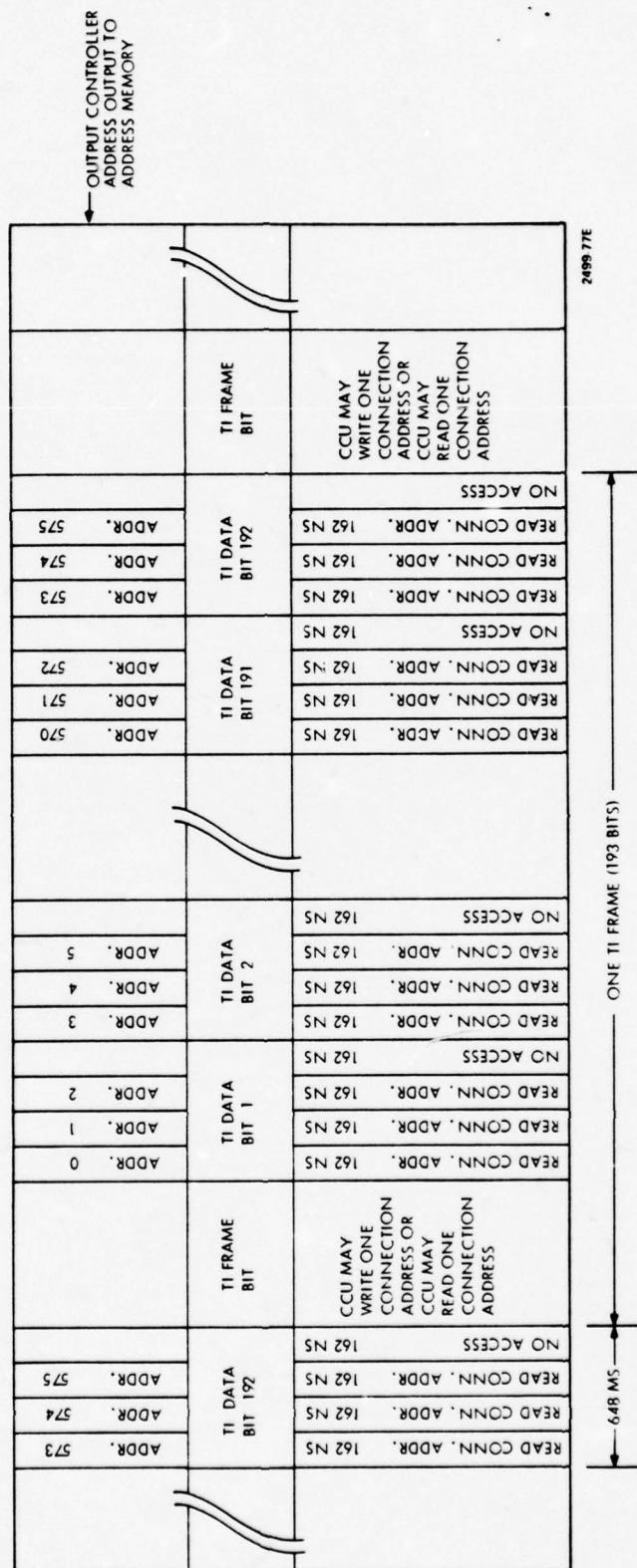


Figure 7-29. Address Memory Operation



c. Output Controller Function - The Output Controller Function provides a sequential address to the Address Memory (0 to 575) during the 192 T1 channel bits. Three addresses are provided during the first 486 ns of a T1 bit. This is illustrated in Figure 7-29. During the T1 frame bit time, it can provide an address (specified by the LOC field of the CCU command) to the Address Memory. The CCU command may specify the following actions on the Address Memory during the T1 frame bit time:

1. Read CA from Address Memory which is stored at address LOC.
2. Write CA into Address Memory at address LOC. Then read the contents of LOC.

In this way, the CCU can update the Address Memory or perform periodic tests on the Address Memory. In either case, the CA read from the Address Memory is clocked into the Connection Address Register.

- d. Address Memory Parity Check Function - Whenever a CA is read from the Address Memory, the Address Memory Parity Check Function checks the parity of the 15-bit CA. If the parity is not odd, the AMP output is set to a logic "1" which also sets the AMP status bit to a "1" in the Parity Status Register. Also, if the parity is bad, the CA is inhibited from being sent to the BDMU. If the parity is odd, the Address Memory Parity Check Function strips off bit CA<sub>14</sub> and routes CA<sub>0</sub>-CA<sub>9</sub> to the BDMU. It also decodes bits CA<sub>10</sub>-CA<sub>13</sub> to determine which BDMU Data Memory is being addressed and sets the enable output for that BDMU Data Memory to a logic "1".
- e. Data Memory Parity Check Encoder Function - The BDMU checks the parity of each 4-bit word read from its Data Memories. If the parity is not odd, then it sets its DMP output to a logic "1". The Data Memory Parity Check Encoder encodes which of the 9 Data Memories was being addressed when the bad parity was detected. The encoding is done with four bits (DMP<sub>0</sub>-DMP<sub>3</sub>). These bits are sent to the Parity Status Register.
- f. Connection Address Register - This hardware element is a 15-bit storage register which stores the CA read from the Address Memory during a T1 frame-bit time. It holds this CA until the CCU requires it. The CCU resets this register after it reads the CA from it by using the CLEAR bit.
- g. Parity Status Register - The Parity Status Register is a 5-bit storage register which stores DMP<sub>0</sub>-DMP<sub>2</sub>, AMP and CMDP for reporting to the CCU. The CCU can reset this register to all "0's" by using the RER command bit.

7.2.2.2.3.2 Partitioning of BOCU Hardware Elements - The BOCU hardware elements will be packaged on one printed circuit card; the BOCU card. Table 7-25 indicates BOCU card requirements versus IFCU size.

TABLE 7-25. BOCU CARD REQUIREMENTS VERSUS IFCU SIZE

NUMBER OF 1.544 MB/S DIGITAL GROUP OUTPUTS FROM THE IFCU	NUMBER OF BOCU CARDS (INCLUDES ONE SPARE)
6	4
12	6
18	8
24	10

7.2.2.2.4 Output Framing and Conversion Unit (OFCU)

7.2.2.2.4.1 OFCU Hardware Description and Operation - The OFCU performs the following functions:

- a. Provides for bit-by-bit comparison of any BOCU data output with the spare BOCU data output for self-test purposes.
- b. Provides the capability to replace any BOCU output with the spare BOCU output.
- c. Converts the 1.544 Mb/s T1 bit streams (3 from each BOCU output) to 1.536 Mb/s or 1.440 Mb/s bit streams.
- d. Demultiplexes the 1.536 Mb/s bit streams into (up to) 12 digital groups.
- e. Demultiplexes the 1.440 Mb/s bit streams into (up to) 10 digital groups.
- f. Inserts the proper TRI-TAC/AUTOSEVOCOM II frame bits into the demultiplexed digital groups under the control of the Framing Unit in the IFCU.

A detailed block diagram of the OFCU is provided in Figure 7-30. This diagram illustrates the OFCU sized for up to 50 output digital groups (demultiplexed from 12 1.544-Mb/s digital groups from

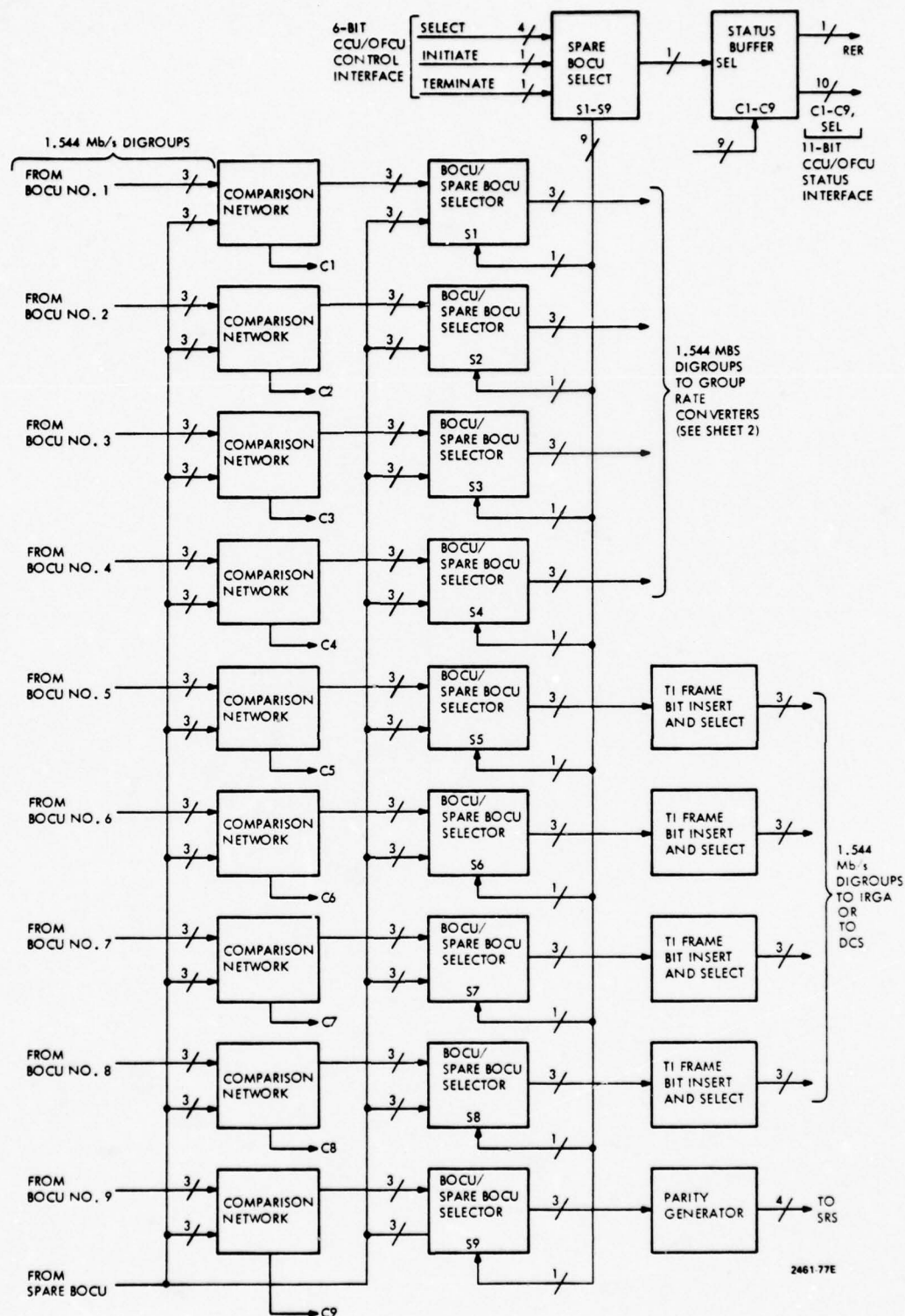


Figure 7-30. OFCU Block Diagram (Sheet 1 of 2)



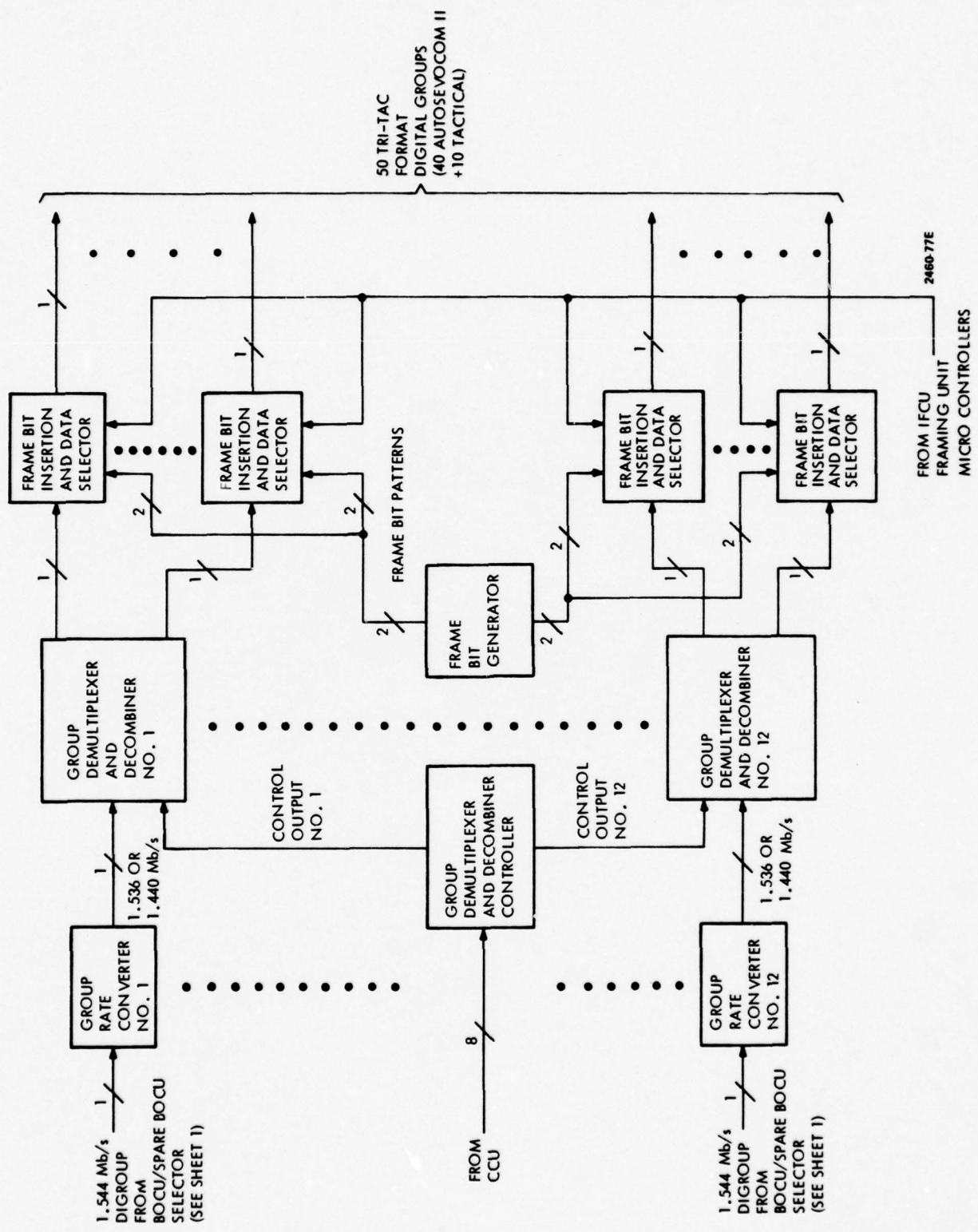


Figure 7-30. OFCU Block Diagram (Sheet 2 of 2)

the BOCUs). The OFCU can be modularly sized in increments of 5 digital group outputs. The OFCU consists of the following hardware elements:

- a. Comparison Network
- b. BOCU/Spare BOCU Selector
- c. Status Buffer Register
- d. Group Demultiplexer and Decombiner
- e. Group Demultiplexer and Decombiner Controller
- f. Group Rate Converter
- g. Frame Bit Insertion Data Selector
- h. Frame Bit Pattern Generator.

These elements are described in detail below.

7.2.2.2.4.1.1 Comparison Network - The Comparison Network is shown in Figure 7-31.

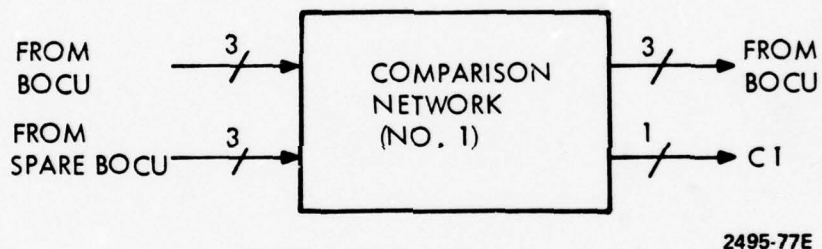


Figure 7-31. Comparison Network

Figure 7-32 illustrates a portion of the BOCU and Spare BOCU parallel 3-bit 1.544 Mb/s bit streams. Each 648 ns, the Comparison Network performs the following comparisons:

$B_0$  with  $B'_0$

$B_1$  with  $B'_1$

$B_2$  with  $B'_2$

If any one of these comparisons results in  $B_n \neq B'_n$ , then the Comparison Network sets its C output to a logic "1" which sets a bit in the Status Buffer Register to a logic "1".

BOCU 3-BIT PARALLEL DATA OUTPUT			648 NS	648 NS	648 NS
			1 BIT	1 BIT	1 BIT
$B_0$					
$B_1$					
$B_2$					
SPARE BOCU 3-BIT PARALLEL DATA OUTPUT			$B'_0$		
			$B'_1$		
			$B'_2$		

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Figure 7-32. Partial BOCU/Spares BOCU Bit Streams

7.2.2.2.4.1.2 BOCU/SPARE BOCU Selector - This hardware element has two inputs:

- a. BOCU Output
- b. Spare BOCU Output.

Under the control of the CCU, this hardware will select either one of the inputs and route it to the Group Rate Converter.

7.2.2.2.4.1.3 Status Buffer Register - This hardware element stores the Comparison Network Status Outputs. In addition, it stores a bit which indicates that the Spare BOCU output has been selected in place of one of the BOCU outputs.

7.2.2.2.4.1.5 Group Rate Converter - The Group Rate Converter is provided to convert 1.544 Mb/s bit streams (from the BOCU/Spare BOCU Selector) down to either 1.536 Mb/s or 1.440 Mb/s bit streams.

7.2.2.2.4.1.6 Group Demultiplexer and Decombiner - This hardware element takes a 1.536 Mb/s or 1.440 Mb/s bit stream from a Group Rate Converter and demultiplexes it into TRI-TAC format digital groups. There are two Group Demultiplexer and Decombiner types. One type accepts a 1.536 Mb/s bit stream and demultiplexes it into  $8,000 \times 2^n$  digital groups. The other type accepts a 1.440 Mb/s bit stream and demultiplexes it into  $9,000 \times 2^n$  digital groups. Table 7-26 illustrates the various output options for the  $8,000 \times 2^n$  Group Demultiplexer and Decombiner. Table 7-27 illustrates the various output options for the  $9,000 \times 2^m$  Group Demultiplexer and Decombiner. The two types utilize the same hardware circuits but use different timing and control signals.

7.2.2.2.4.1.7 Group Demultiplexer and Decombiner Controller - This hardware element controls the order in which the multiplexed digital groups are decombed. This hardware element controls up to 12 Group Demultiplexers and Decombiners and receives control commands from the CCU.

7.2.2.2.4.1.8 Frame Bit Insertion Data Selector - During the frame bit time of the TRI-TAC formatted digital group, this hardware selects the output of the Frame Bit Pattern Generator and hence inserts a frame bit into the digital group bit stream. The output of this hardware element is a complete and fully framed TRI-TAC formatted digital group. The data bits can also be set to all zeroes under control of the Framing Unit Microcontroller in the IFCU.



TABLE 7-26. VARIOUS DIGROUP OUTPUT OPTIONS FOR THE  
8,000 x 2<sup>n</sup> GROUP MULTIPLEXER AND COMBINER

128 KB/S	256 KB/S	512 KB/S	1024 KB/S	1536 KB/S	CASE NO.
0	0	1	1	0	1
0	2	0	1	0	2
2	1	0	1	0	3
4	0	0	1	0	4
0	0	3	0	0	5
0	2	2	0	0	6
2	1	2	0	0	7
4	0	2	0	0	8
0	4	1	0	0	9
2	3	1	0	0	10
4	2	1	0	0	11
6	1	1	0	0	12
0	6	0	0	0	13
2	5	0	0	0	14
4	4	0	0	0	15
6	3	0	0	0	16
8	2	0	0	0	17
10	1	0	0	0	18
12	0	0	0	0	19
0	0	0	0	1	20

TABLE 7-27. VARIOUS DIGROUP OUTPUT OPTIONS FOR THE  
9,000 x 2<sup>m</sup> GROUP MULTIPLEXER AND COMBINER

144 KB/S	288 KB/S	576 KB/S	1152 KB/S	CASE NO.
0	1	0	1	1
2	0	0	1	2
0	1	2	0	3
0	3	1	0	4
2	2	1	0	5
4	1	1	0	6
6	0	1	0	7
0	5	0	0	8
2	4	0	0	9
4	3	0	0	10
6	2	0	0	11
8	1	0	0	12
10	0	0	0	13

7.2.2.2.4.1.9 Frame Bit Pattern Generator - This hardware element generates two frame bit patterns: 101010.... and 1111111.... These patterns are provided to each Frame Bit Insertion Data Selector.

7.2.2.2.4.2 Partitioning of the OFCU Hardware Elements - The OFCU hardware is partitioned onto four printed circuit card types as follows:

- a. OFCU Card No. 1
- b. OFCU Card No. 2
- c. OFCU Card No. 3
- d. OFCU Card No. 4.

OFCU Card No. 1 services up to 12 1.544-Mb/s digital group inputs from four BOCUs. OFCU Card No. 2 services up to 12 1.544-Mb/s digital group inputs from four BOCUs. Each OFCU Card No. 3 services one 1.544-Mb/s digital group input from a BOCU. OFCU Card No. 4 services up to 12 1.544-Mb/s digital group inputs to the OFCU. Figure 7-32A illustrates

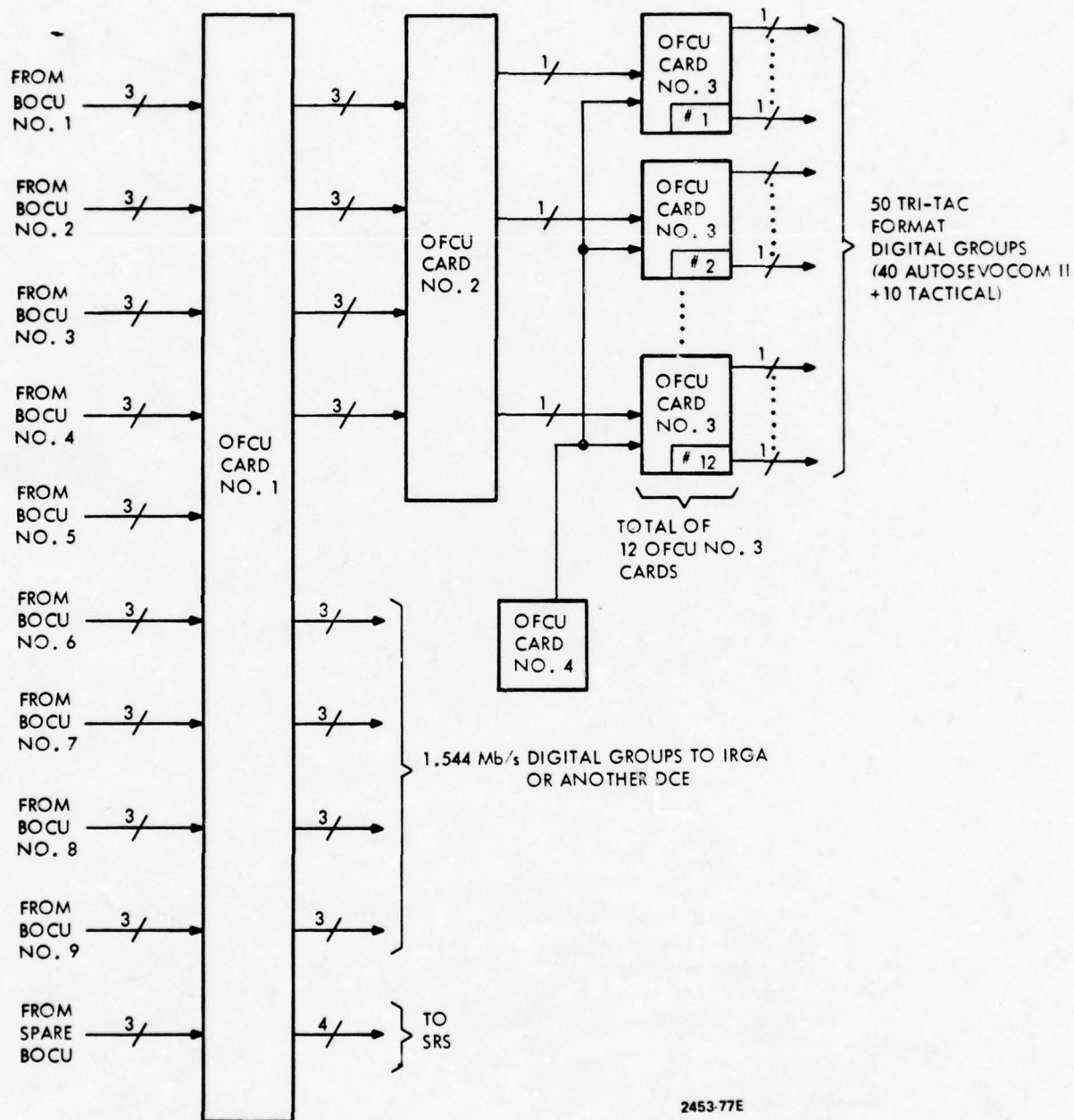


Figure 7-32A. Interconnection of OFCU Cards

the interconnection of OFCU cards for the maximum size OFCU of 12 1.544-Mb/s input digroups and 50 output TRI-TAC format digroups. Table 7-28 indicates the number of each card type versus the basic IRGB size.

Referring to Figure 7-30, the OFCU hardware elements are partitioned among the four OFCU card types as follows:

- a. OFCU Card No. 1 - This card contains the following hardware elements:
  1. 8 Comparison Networks
  2. 8 BOCU/Spare BOCU Selectors
  3. Status Buffer Register
  4. Parity Generator
  5. 12 T1 Frame Bit Insertion Selectors.
- b. OFCU Card No. 2 - This card contains 12 Group Rate Converters.
- c. OFCU Card No. 3 - This card contains the following hardware elements:
  1. One Group Demultiplexer and Decombiner
  2. Twelve Frame Bit Insertion Data Selectors.
- d. OFCU Card No. 4 - This card contains the following hardware elements:
  1. Frame Pattern Generator
  2. Group Demultiplexer and Decombiner Controller.

7.2.2.2.5 Subchannel Reassignment Subgroup (SRS) - The SRS provides the IRGB with the capability to reassign Tactical/AUTOSEVOCOM II overhead subchannels. The SRS architecture is similar to the BDMU/BOCU architecture. The SRS is comprised of two major components:

- a. S Data Memory Unit (SDMU)
- b. S Output Control Unit (SOCU).

The SRS also includes a spare SDMU and a spare SOCU. The SDMU and SOCU are described in detail below. A block diagram of the SR is provided in Figure 7-33.

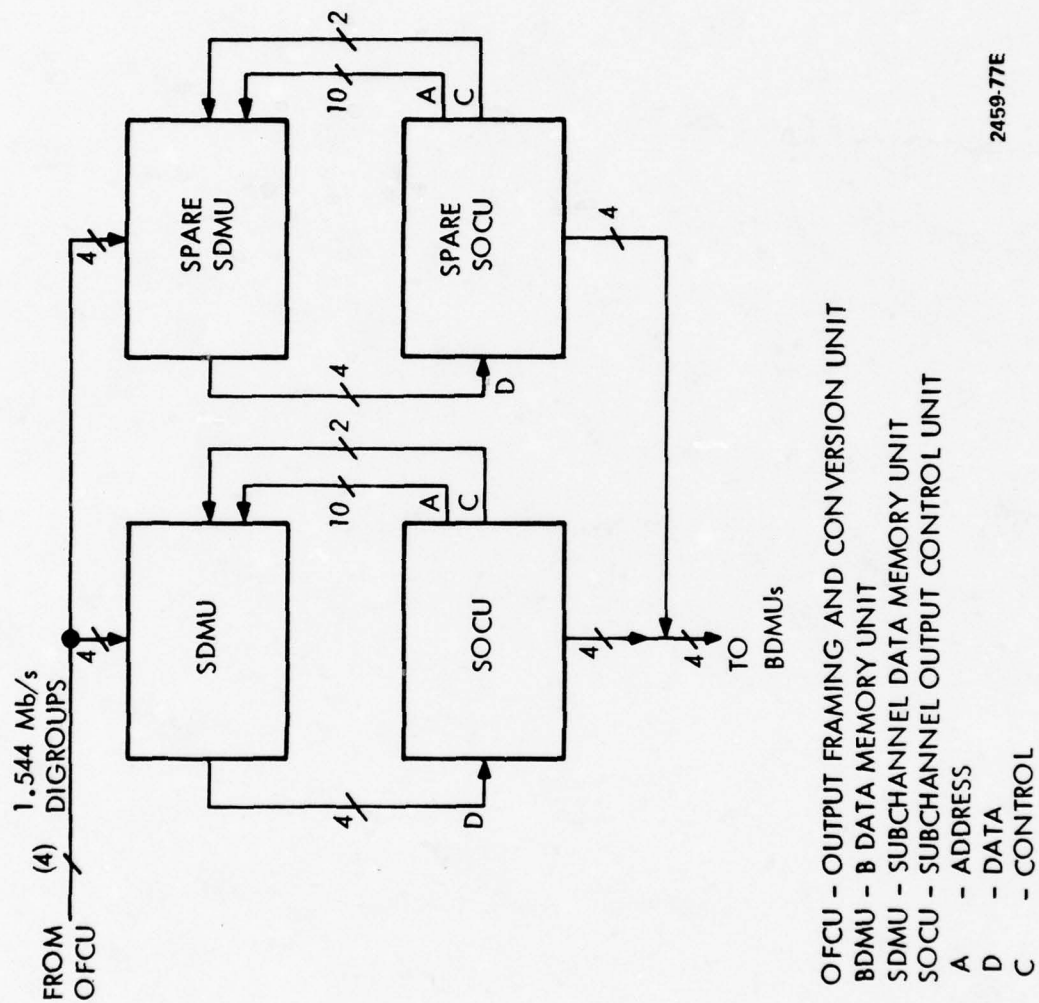
Three 1.544-Mb/s digroups from the OFCU each carry up to 96 TRI-TAC overhead channels. The SRS can handle up to 96 x 3 or 288 TRI-TAC format overhead channels. Since each overhead channel contains 8 subchannels, the SRS can reassign a maximum of 2304 subchannels.



TABLE 7-28. OFCU CARD REQUIREMENTS VERSUS OFCU SIZE

NUMBER OF 1.544 MB/S DIGITAL GROUP FROM BOCU(S)	NUMBER OF OFCU NO. 1 CARDS	NUMBER OF OFCU NO. 2 CARDS	NUMBER OF OFCU NO. 3 CARDS	NUMBER OF OFCU NO. 4 CARDS
① 6	1	1	3	1
② 12	1	1	6	1
③ 18	1	1	9	1
④ 24	1	1	12	1

- NOTES: ① Total of 15 output digital groups.  
 ② Total of 25 output digital groups.  
 ③ Total of 40 output digital groups.  
 ④ Total of 50 output digital groups.



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Figure 7-33. Subchannel Reassignment Subgroup Block Diagram

7.2.2.2.5.1 S Data Memory Unit (SDMU) Hardware Description - The SDMU architecture and operation are almost identical to those of the BDMU (refer to Section 7.2.2.2.2).

The SDMU is the heart of the SRS in that it is the element that performs the reassignment of subchannels (under the control of the SOCU). Each SDMU has three 1.544-Mb/s overhead channel bit streams.

A detailed block diagram of the SDMU is provided in Figure 7-34. The SDMU consists of the following hardware elements:

- a. Data Memory
- b. Read/Write Address Selector
- c. Data Memory Parity Check
- d. Selector
- e. Parity Generator.

The SDMU differs from the BDMU in that it has only Data Memory. The SDMU hardware elements are described below.

- a. Data Memory - The Data Memory is a 768 x 4-bit Random Access Memory (RAM). This memory stores eight frames worth of 288 16-kb/s overhead channels or 2304 subchannels (derived from 288 16-kb/s overhead channels). In addition, a parity bit is stored for each 3-bit word of subchannels.
- b. Data Memory Parity Check - This hardware element strips off the three subchannel bits in a 4-bit Data Memory word and passes these bits to the Selector. It also checks the 4-bit word for odd parity and sets its PE line to a logic "1" if odd parity is not present.
- c. Selector - The Selector performs the function of routing each one of the three subchannel bits to any of the three SDMU output bit streams.
- d. Read/Write Address Selector - This element selects an address generated by an internal counter during the first 1/4 of the T1 bit time and then switches to the address output of the SOCU for the remaining 3/4 of a T1 bit time.
- e. Parity Generator - This element adds a fourth (parity) bit to the 3-bit word from the Selector such that the 4-bit word has odd parity.

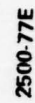


Figure 7-34. SDMU Block Diagram



7.2.2.2.5.2 S Output Control Unit (SOCU) Hardware Description and Operation - The SOCU controls the SDMU to perform subchannel reassignment. The SOCU interfaces directly with the Central Control Unit (CCU) in the Common Equipment Group.

-- A detailed block diagram of the SOCU is provided in Figure 7-35. The SOCU consists of the following hardware elements:

- a. Command Parity Check Function - The CCU controls the SOCU via a 31-bit parallel command interface. CCU commands are received by the Command Parity Check Function. Figure 7-36 illustrates the various fields in the CCU command. The Command Parity Check Function checks the parity of the 31-bit command. If the 31-bit command does not display odd parity, then the CMDP output is set to a logic "1" and the COMP status bit is set to a "1" in the Parity Status Register. Also, the command is inhibited from acting on other SOCU hardware by disabling the RCA' and WCA' outputs. The Command Parity Check Function also strips the CA and LOC fields off the command and sends these to the Address Memory and the Output Controller Function, respectively.
- b. Address Memory - The Address Memory is a 2304 x 13-bit RAM. It stores 2304 connection addresses (CA<sub>0</sub>-CA<sub>12</sub>). The connection address determines which of the 2304 subchannels will be read from the SDMU Data Memory. The subchannel reassignment function of the SRS resides in the sequence of connection addresses stored in the Address Memory. The connection addresses are written into the Address Memory by the CCU; one connection address is written during each T1 frame bit. During a T1 data bit time, there are three read accesses performed on the Address Memory. This is illustrated in Figure 7-37. The Address Memory may be read from or written into once during each T1 frame bit time under the control of the CCU.
- c. Output Controller Function - The Output Controller Function provides sequential addresses to the Address Memory (0 to 2303) during 768 T1 channel bits. Three addresses are provided during the first 486 ns of the T1 bit. This is illustrated in Figure 7-37. During the T1 frame bit time, it can provide an address (specified by the LOC field of the CCU command) to the Address Memory. The CCU command may specify the following actions on the Address Memory during the T1 frame bit time:
  1. Read CA from Address Memory which is stored at address LOC.
  2. Write CA into Address Memory at address LOC. Then read the contents of LOC.

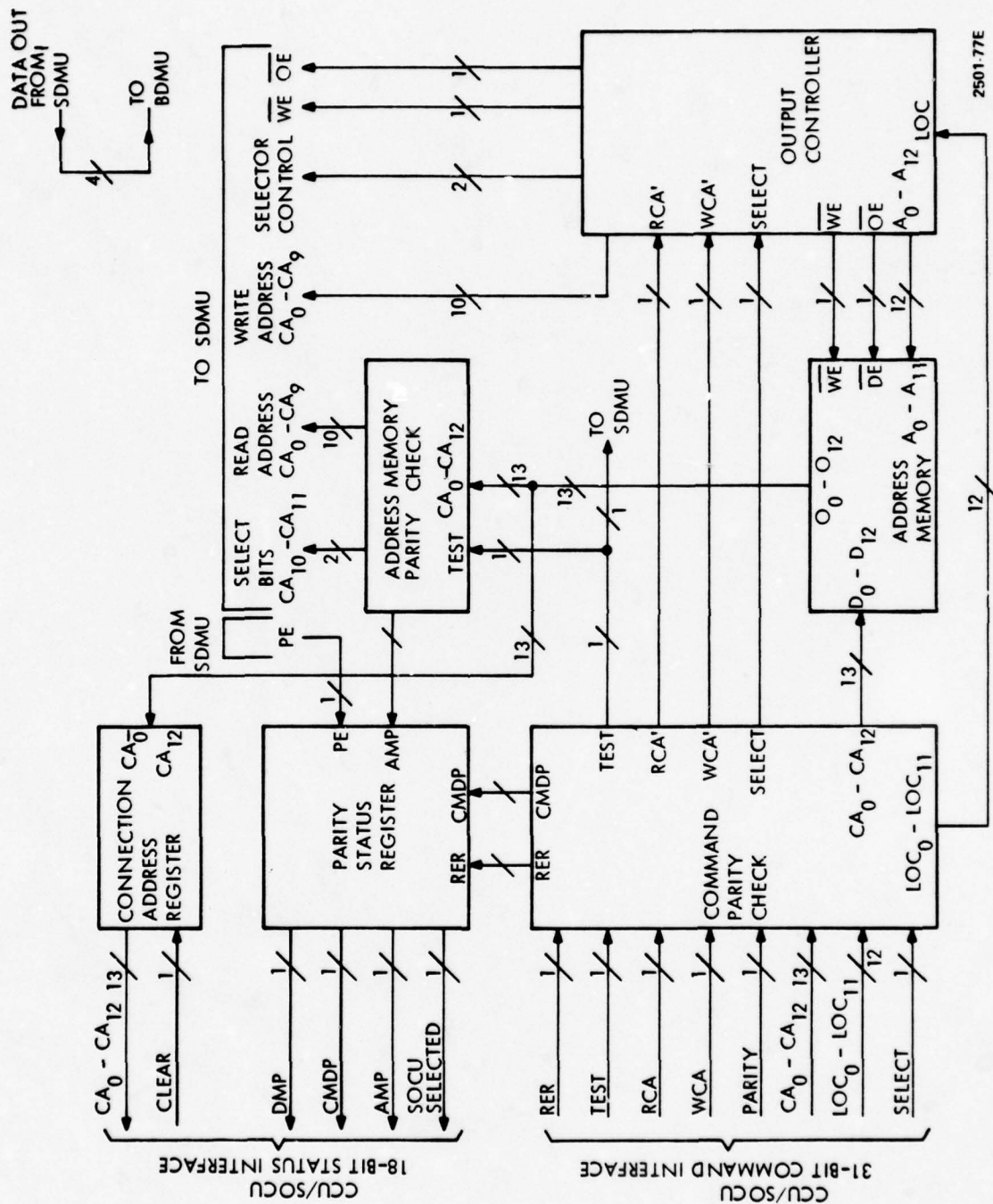
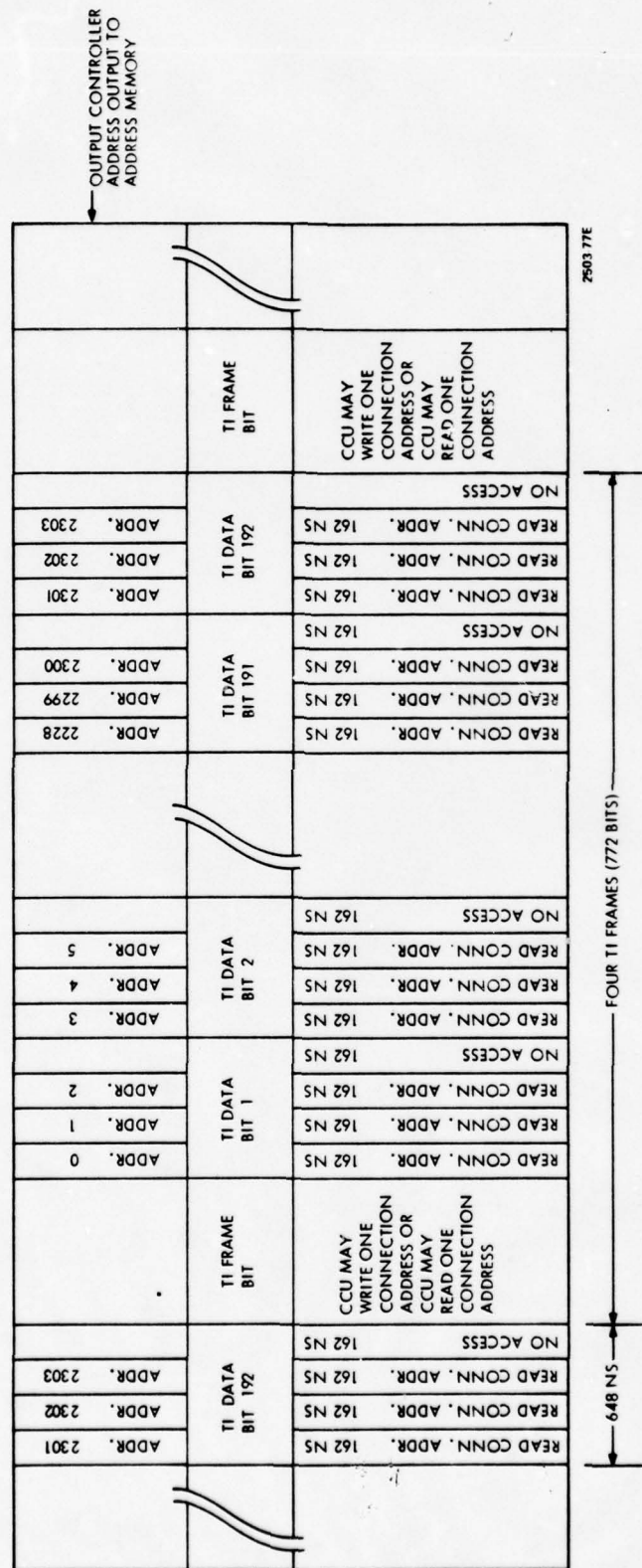


Figure 7-35. SOCU Block Diagram

Figure 7-36. CCU Command Format for SOCU Control





In this way, the CCU can update the Address Memory or perform periodic tests on the Address Memory. In either case, the CA read from the address Memory is clocked into the Connection Address Register.

- d. Address Memory Parity Check Function - Whenever a CA is read from the Address Memory, the Address Memory Parity Check Function checks the parity of the 13-bit CA. If the parity is not odd, the AMP output is set to a logic "1" which also sets the AMP status bit to a "1" in the Parity Status Register. Also, if the parity is bad, the CA is inhibited from being sent to the SDMU. If the parity is odd, the Address Memory Parity Check Function strips off bit CA<sub>12</sub> and routes CA<sub>0</sub>-CA<sub>9</sub> to the SDMU. It also routes bits CA<sub>10</sub> and CA<sub>11</sub> to the SDMU Selector.
- e. Connection Address Register - This hardware element is a 13-bit storage register which stores the CA read from the Address Memory during a frame bit time. It holds this CA until the CCU requires it. The CCU resets this register after it reads the CA from it by using the CLEAR bit.
- f. Parity Status Register - The Parity Status Register is a 4-bit storage register which stored DMP, SOCU SELECTED, AMP and CMDP for reporting to the CCU. The CCU can reset this register to all "0's" by using the RER command bit.

#### 7.2.2.2.5.3 Partitioning of SRS Hardware Elements

7.2.2.2.5.3.1 SDMU - The SDMU hardware elements will be packaged on one printed circuit card; the SDMU Card. The SOCU hardware elements will be packaged on one printed circuit card; the SOCU Card. Table 7-29 indicates the SDMU and SOCU Card requirements versus IRGA size.

TABLE 7-29. SDMU/SOCU CARD REQUIREMENTS VERSUS IFCU SIZE

NUMBER OF 1.544 MB/S DIGITAL GROUP OUTPUTS FROM IFCU	NUMBER OF SDMU CARDS (INCLUDES ONE SPARE)	NUMBER OF SOCU CARDS (INCLUDES ONE SPARE)
6	2	2
12	2	2
18	2	2
24	2	2

#### 7.2.2.3 Common Equipment Group (CEG)

A block diagram of the CEG is shown in Figure 7-38.

The CEG has the following functional capabilities:

- a. Provides the command/status interface between System Control and all the DCE groups, namely the IRGA and IRGB
- b. Provides the command/status interface between a local terminal and all the DCE groups
- c. Provides fault detection and isolation for the CEG, IRGA and IRGB
- d. Provides all DCE timing signals and clocks
- e. Provides power to all DCE groups.

The CEG comprises three basic functional hardware units:

- a. Central Control Unit (CCU)
- b. Master Timing Unit (MTU)
- c. Power Supply Unit (PSU).

Figure 7-39 illustrates the CEG in more detail.

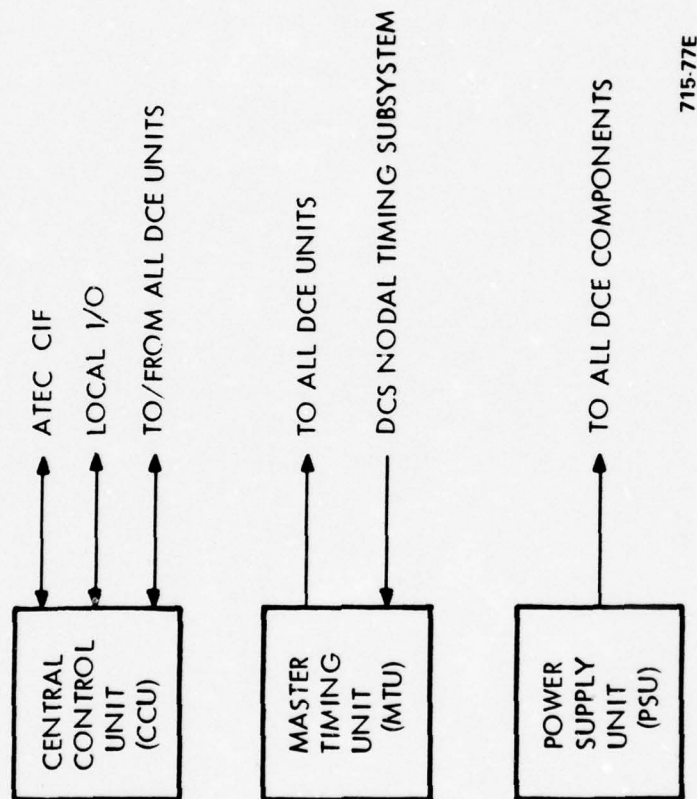
**7.2.2.3.1 Central Control Unit (CCU)** - The CCU is a complete, special purpose microcomputer based on the 8080A microprocessor family of components. The CCU consists of:

- a. Central Processor Unit (CPU) Element
- b. Memory Element
- c. I/O Element.

These hardware elements are described in detail in the following sections.

A detailed block diagram of the CCU is provided in Figure 7-40. There are three busses that interconnect the three CCU elements:

- a. Data Bus - A bi-directional path on which data can flow between the CPU and Memory or between the CPU and I/O.
- b. Address Bus - A uni-directional group of lines that identify a particular Memory location or I/O device.



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Figure 7-38. Common Equipment Group

CENTRAL CONTROL UNIT	MASTER TIMING UNIT	POWER SUPPLY UNIT
(1) CCU CPU CARD (1) CCU I/O CARD NO. 1 (1) CCU I/O CARD NO. 2 (1) CCU I/O CARD NO. 3	(1) TIMING STANDARD CONTROLLER CARD (1) TIMING STANDARD SYNTHESIZER CARD (1) DISTRIBUTION DRIVER CARD (1) PRECISION VCO SUBASSEMBLY NOTE } 3 CARDS 1 } 1 SUBASSEMBLY	+5V NOTE 2 -5V NOTE 3 +12V NOTE 3 -12V NOTE 2 +15V NOTE 3 -15V NOTE 3

- NOTES: 1. NUMBER OF CARDS DOES NOT DEPEND ON DCE SIZE.
2. OUTPUT CURRENT DEPENDS ON DCE SIZE.
3. OUTPUT CURRENT DOES NOT DEPEND ON DCE SIZE.
4. NUMBER OF CARDS DEPENDS ON DCE CONFIGURATION.

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Figure 7-39. DCE Common Equipment Group (CEG)



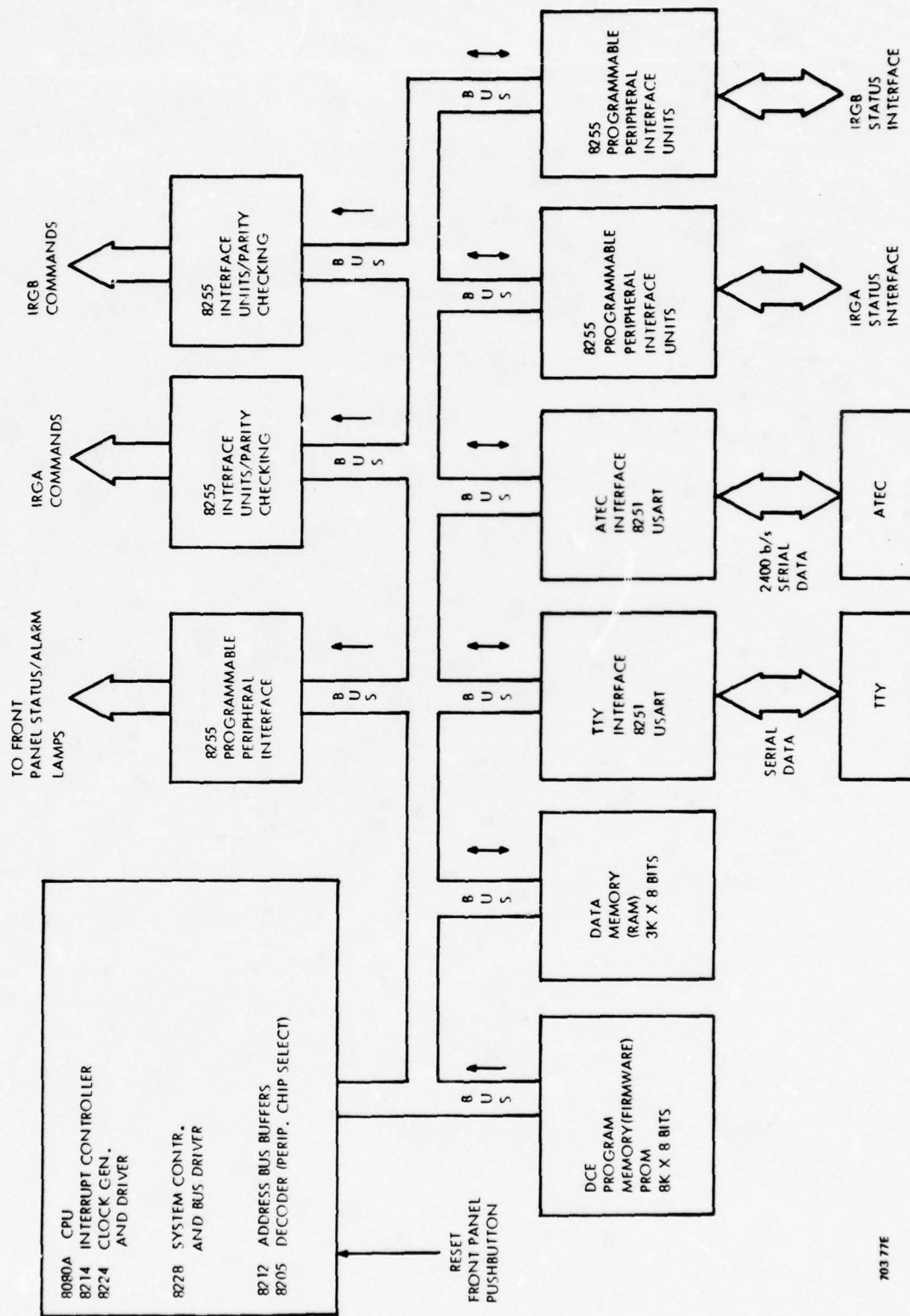


Figure 7-40. Central Control Unit Block Diagram

- c. Control Bus - A uni-directional set of signals that indicate the type of CCU activity currently in process. The types of CCU activities are:

1. Memory or I/O Read
2. Memory or I/O Write
3. Interrupt Acknowledge.

7.2.2.3.1.1 CPU Element Description and Operation - The CPU Element, in conjunction with the Scratchpad Memory (RAM) of the Memory Element and the I/O Element, executes the DCE software algorithms which are contained in firmware (Programmable Read Only Memory - PROM). The CPU Element contains the CPU, system timing and interface circuitry to Memory and I/O devices. Specifically the CPU element consists of:

- a. CPU - The CPU consists of an 8080A single chip, 8-bit microprocessor. The 8080A CPU includes the following functional items:
  1. Register array and address logic
  2. Arithmetic and Logic Unit (ALU)
  3. Instruction register and control section
  4. Bi-directional, 3-state data bus buffer.
- b. Interrupt Controller - The Interrupt Controller is based on the 8214 priority interrupt control unit chip. The Interrupt Controller provides overall management of the CCU interrupt system. It accepts interrupt requests from the I/O devices, determines which request has the highest priority, determines whether the incoming request has a higher priority than the interrupt level currently being serviced (if any), and it then issues an interrupt to the 8080A if the new priority level is higher or no interrupt is currently being serviced. The Interrupt Controller also provides an interrupt vector for each I/O device so that the program counter in the 8080A can be "vectored" to the starting address of the interrupt service routine for the particular I/O device.
- c. Clock Generator and High Level Driver - This hardware element consists of an 8224 single chip, clock generator and driver for the 8080A CPU and a crystal. In addition to other functions, this element provides the phase 1 and phase 2 clocks for the 8080A, the power-up reset for the 8080A, and a phase 2 clock output for external system timing on the CCU.
- d. System Controller and Bus Driver - This hardware consists of the 8228 single chip, system controller and bus driver. It generates all signals required to interface the 8080A CPU with the Memory Element and the

I/O Element. It also provides for buffering of the 8080A 8-bit data bus so that a large number of chips may be placed on the data bus (including PROM, RAM and I/O devices).

- e. Address Bus Buffer - The Address Bus Buffer isolates the 8080A 16-bit address bus so that all PROM, RAM and I/O devices can be connected to that bus.
- f. Decoder - The Decoder expands the address bus so that many PROM, RAM and I/O devices can be individually addressed. It produces a chip select line for each peripheral device to be addressed by the 8080A CPU.

7.2.2.3.1.2 Memory Element Description and Operation - The Memory Element provides RAM storage for the 8080A CPU and it also stores the DCE software algorithms as firmware in PROM. The DCE Program Memory (firmware) is contained in a 8k x 8-bit Programmable Read Only Memory (PROM). The Data Memory is contained in a 3k x 8-bit Read/Write Memory (RAM). The CCU utilizes a Memory Mapped I/O concept in which the I/O devices are treated the same as memory locations. With this method, all 8080A instructions that can be used to operate on memory locations can be used in I/O. This provides an increase in overall processing speed and provides for reduced firmware.

7.2.2.3.1.3 I/O Element Description and Operation - The I/O Element contains a System Control communications interface. This interface provides a full-duplex I/O port operating at a data rate of 150 baud. The interface will provide for transmission of ASCII status characters from the 8080A CPU to System Control and for reception of ASCII command characters from System Control to the 8080A CPU.

The I/O Element also contains an interface for a local TTY. The TTY will be used for local control of the DCE.

In addition, the I/O Element contains the following interface hardware:

- a. Control Panel Interface for allowing the CCU to control Status and Alarm lamps on the Control Panel.
- b. A command interface with the IRGA. This interface buffers commands to the IRGA, checks the parity of these commands and, if bad parity is detected, reports the fault condition to the 8080A CPU and disables commands from being sent to the IRGA.
- c. A command interface with the IRGB. See item b. for details.
- d. A status interface with the IRGA.
- e. A status interface with the IRGB.



The System Control and TTY communications interfaces each consist of the 8251 single-chip programmable communication interface. The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) chip.

The remaining interfaces utilize the 8255 programmable peripheral interface chip.

As an option, an additional 8255 chip could be added to the CCU to provide an interface to a mini-floppy disk controller and drive unit. A chip select line for this purpose has been provided for by the Decoder in the CPU Element.

7.2.2.3.1.4 Partitioning of CCU Hardware Elements - The CCU hardware is partitioned onto four printed circuit card types as follows:

a. CCU Central Processor Unit Card - This card includes the following hardware:

1. CPU Element
2. Memory Element: 3k x 8-bit RAM, 8k x 8-bit EPROM
3. Part of the I/O Element: System Control Communications Interface, TTY Communications Interface, Control Panel Interface.

The remaining portions of the I/O Element are included on CCU I/O Card No. 1, No. 2 and No. 3.

b. CCU I/O Card No. 1 - This card contains the following portion of the I/O Element: IRGA Command Interface.

c. CCU I/O Card No. 2 - This card contains the following portion of the I/O Element: IRGB Command Interface.

d. CCU I/O Card No. 3 - This card contains the following portions of the I/O Element:

1. IRGA Status Interface
2. IRGB Status Interface.

The actual CCU card types required for a particular DCE installation depends on which groups the CCU must interface with. Table 7-30 summarizes CCU card requirements.



TABLE 7-30. CCU CARD REQUIREMENTS

DCE CONFIGURATION	CCU CPU CARD	CCU CARDS REQUIRED		CCU I/O CARD NO. 3
		CCU I/O CARD NO. 1	CCU I/O CARD NO. 2	
IRGA Only	1	1	0	1
IRGB Only	1	0	1	1
IRGA and IRGB	1	1	1	1

7.2.2.3.2 Master Timing Unit (MTU) - A block diagram of the MTU is provided in Figure 7-41.

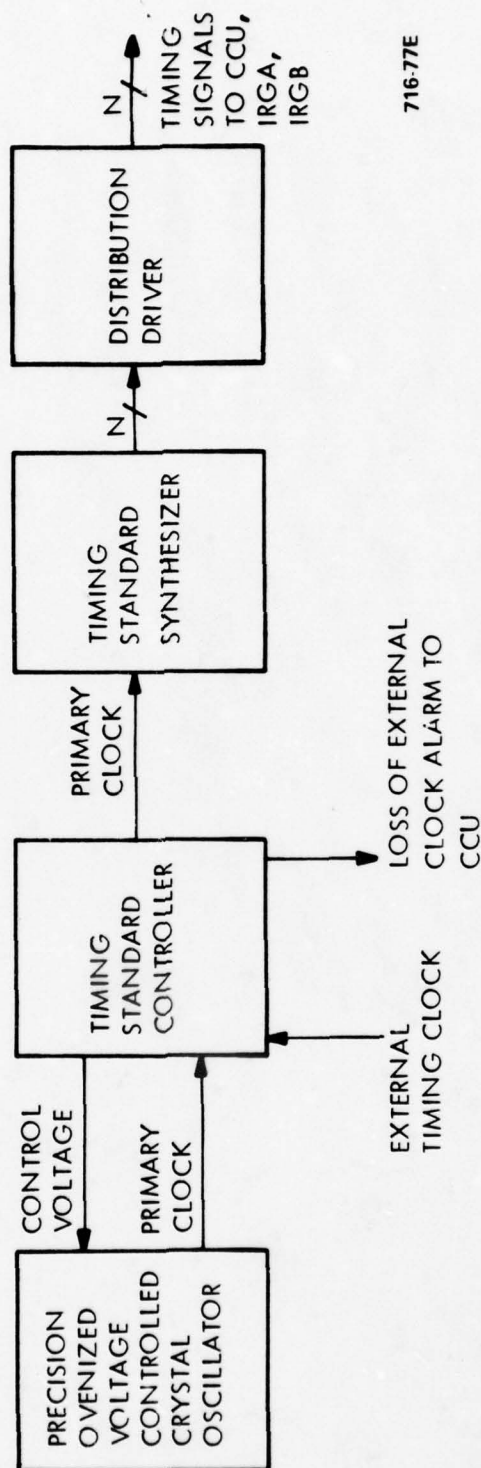
The MTU provides accurate, stable timing signals for the IRGA, IRGB and CCU by slaving to the DCS Nodal Timing Subsystem. The MTU also provides a free running capability in the event of a loss of the external clock signal from the DCS Nodal Timing Subsystem. The MTU automatically detects a loss of the external clock and switches to free running operation.

The MTG consists of three printed circuit cards and one precision ovenized voltage controlled oscillator subassembly which, when interconnected, provide a source of clock frequencies which are used throughout the DCE. The timing standard produces a clock which is used to synthesize the various DCE clock signals required. These frequencies are distributed via digital line drivers to the user cards.

The timing standard is a precision voltage controlled quartz crystal oscillator (ovenized) which is slaved (phase locked) to an external clock from the DCS Nodal Timing Subsystem. The timing standard thereby acquires the stability of the external clock. The timing standard is capable of standalone operation with a stability of  $\leq 5 \times 10^{-10}$  parts per day in the event of a loss of the external clock.

7.2.2.3.2.1 Partitioning of MTU Hardware - The MTU consists of three printed circuit cards and one subassembly as follows:

- a. Precision Ovenized Voltage Controlled Quartz Crystal Oscillator Subassembly
- b. Timing Standard Controller Card



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Figure 7-41. Master Timing Unit (MTU) Block Diagram

- c. Timing Standard Synthesizer Card
- d. Distribution Driver Card.

All of these cards and the subassembly are required regardless of the DCE configuration.

7.2.2.3.3 Power Supply Unit (PSU) - The PSU provides the total DCE power supply requirements. The PSU supplies the following voltages to the IRGA, IRGB and CCU and MTU:

+5V, -5V, +12V, -12V, +15V, -15V.

The +5V and -12V output current requirements depend on the size of the IRGA and IRGB. The -5V, +12V and +15V output current requirements are independent of DCE size or configuration.

The following tables present the various DCE power requirements:

- a. Table 7-31: Power Requirements of IRGA Card Types
- b. Table 7-32: Power Requirements of IRGB Card Types
- c. Table 7-33: CEG Power Requirements
- d. Table 7-34: IRGA Power Requirements Versus IRGA Size
- e. Table 7-35: IRGB Power Requirements Versus IRGB Size.

The PSU will consist of modular power supplies such that the capacity of the PSU can be modularly matched to the power requirements of any particular size and configuration DCE.

### 7.2.3 Physical Description

#### 7.2.3.1 DCE Printed Circuit Card

All DCE printed circuit cards will utilize the same type printed wiring board.

Figure 7-42 illustrates the printed wiring board. The board uses a 112 pin edge connector plug. Most of the boards will be of the multilayer type with two internal signal wiring planes and power and ground planes on the board's outside surfaces.

#### 7.2.3.2 DCE Printed Circuit Card Nest

The DCE, depending on its size and configuration, will utilize one or more nests to hold the printed circuit cards. Each nest will contain 41 card slots and will hold up to 41 printed circuit cards. Each slot provides card guides to hold the card in place. In addition, the slot provides a connector receptacle with a 112-pin connector jack which mates with the 112 pin connector plug on the printed wiring board.

TABLE 7-31. SUMMARY OF DCE IRGA CARD POWER REQUIREMENTS

CARD TYPE	+5 VOLTS		-12 VOLTS	
	I TYP (mA)	P TYP (W)	I TYP (mA)	P TYP (W)
ADMU	1351.8	6.76		
AOCU CONTROLLER	506.6	2.53		
AOCU ADDRESS MEMORY	786.8	3.93		
IFU FRAMING UNIT	1377.3	6.89		
IFU DIGROUP BUFFER	1215.1	6.08	53.0	0.64
IFU CHANNEL SELECTOR	1470.8	7.35		
IFU FRAME ALIGNMENT	2230.6	11.20		
OFU CARD NO. 1	209.9	1.05		
OFU CARD NO. 2	74.8	.37		
OFU CARD NO. 3	800.4	4.00		

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TABLE 7-32. SUMMARY OF DCE IRGB CARD POWER REQUIREMENTS

CARD TYPE	+5 VOLTS		-12 VOLTS	
	I TYP (mA)	P TYP (W)	I TYP (mA)	P TYP (W)
BDMU	745.0	3.73		
BOCU	1394.0	6.97		
IFCU FRAMING UNIT	1377.3	6.89		
IFCU DIGROUP BUFFER	1215.1	6.08	53.0	0.64
IFCU FRAME ALIGNMENT	1215.1	6.08	53.0	0.64
IFCU MULTIPLEXER	2216.0	11.08	63.6	0.76
IFCU MUX CONTROLLER	900.0	4.50		
OFCU CARD NO. 1	254.2	1.27		
OFCU CARD NO. 2	2130.0	10.65		
OFCU CARD NO. 3	2280.0	11.40		
OFCU CARD NO. 4	900.0	4.50		
SDMU	259.7	1.30		
SOCU	3179.7	15.90		

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TABLE 7-33. SUMMARY OF DCE CEG POWER REQUIREMENTS

(A) CENTRAL CONTROL UNIT (CCU)

CARD TYPE	+5 VOLTS		-5 VOLTS		+12 VOLTS	
	I TYP (mA)	P TYP (W)	I TYP (mA)	P TYP (W)	I TYP (mA)	P TYP (W)
CCU CPU CARD	2309.0	11.55	0.01	NEGLIGIBLE	58.0	0.70
CCU I/O CARD NO. 1	1189.6	5.95				
CCU I/O CARD NO. 2	1414.4	7.07				
CCU I/O CARD NO. 3	680.0	3.40				

(B) MASTER TIMING UNIT (MTU)

+15V @ 0.4A ( 6.0W)  
 -15V @ 0.05A ( 0.75W)  
 + 5V @ 3.0A (15.0W)  
 - 5V @ 0.1A ( 0.5W)

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TABLE 7-34. DCE IRGA POWER REQUIREMENTS VERSUS NUMBER OF  
1.544 MB/S DIGROUP INPUTS

NUMBER OF DIGROUP INPUTS	IFU POWER REQUIRED (WATTS)	DMU POWER REQUIRED (WATTS)	OCU POWER REQUIRED (WATTS)	OFU POWER REQUIRED (WATTS)	TOTAL POWER REQUIRED (WATTS)
32	+5V 143	14	13	17	+5V 187
	-12V 4				-12V 4
64	+5V 265	41	19	33	+5V 358
	-12V 8				-12V 8
96	+5V 408	81	26	49	+5V 564
	-12V 13				-12V 13
128	+5V 529	135	32	66	+5V 762
	-12V 17				-12V 17
160	+5V 651	203	39	82	+5V 975
	-12V 20				-12V 20
192	+5V 782	284	45	98	+5V 1209
	-12V 25				-12V 25

NOTE: ALL POWER REQUIREMENTS ARE +5V UNLESS OTHERWISE INDICATED.

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TABLE 7-35. DCE IRGB POWER REQUIREMENTS VERSUS NUMBER OF IFCU OUTPUT DIGROUPS

NUMBER OF IFCU OUTPUT DIGROUPS	IFCU POWER REQUIRED (WATTS)	BDMU POWER REQUIRED (WATTS)	BOCU POWER REQUIRED (WATTS)	OFCU POWER REQUIRED (WATTS)	SRS POWER REQUIRED (WATTS)	TOTAL POWER REQUIRED (WATTS)
6 NOTE 1.	+5V 80	20	42	51	34	+5V 227
	-12V 2					-12V 2
12 NOTE 2.	+5V 125	31	63	85	34	+5V 338
	-12V 3					-12V 3
18 NOTE 3.	+5V 182	41	85	119	34	+5V 461
	-12V 5					-12V 5
24 NOTE 4.	+5V 227	51	106	153	34	+5V 571
	-12V 6					-12V 6

NOTE 1. A TOTAL OF 15 INPUT TACTICAL PLUS AUTOSEVOCOM II TRUNK GROUPS TO IFCU.  
 2. A TOTAL OF 25 INPUT TACTICAL PLUS AUTOSEVOCOM II TRUNK GROUPS TO IFCU.  
 3. A TOTAL OF 40 INPUT TACTICAL PLUS AUTOSEVOCOM II TRUNK GROUPS TO IFCU.  
 4. A TOTAL OF 50 INPUT TACTICAL PLUS AUTOSEVOCOM II TRUNK GROUPS TO IFCU.

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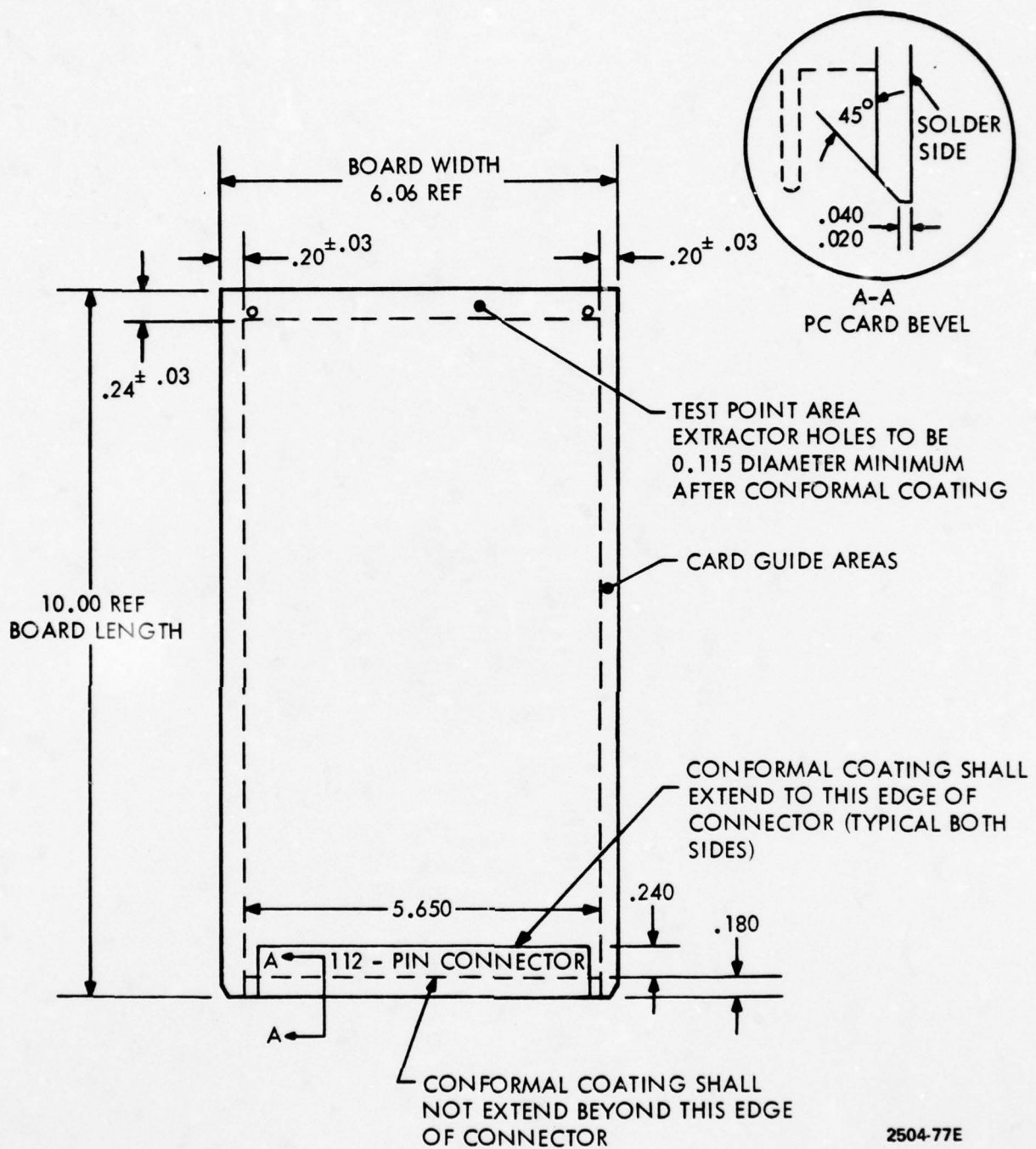


Figure 7-42. Standard Card Type for the DCE

The nest is designed to be mounted in the standard commercial rack used to house the DCE.

The rear of the nest provides 112 wire-wrap pins for each card slot plus a power and ground plane.

Figure 7-42A illustrates the basic DCE nest modules used to build up any DCE configuration. The IRGA, depending on its size, requires one to six IRGA nest modules. The IRGB, depending on its size, requires either one IRGB nest module A or one module A and one module B. The CEG requires one CEG nest module.

#### 7.2.3.3 DCE Equipment Assembly

Figure 7-42B illustrates a typical DCE equipment assembly. This particular DCE is sized as follows:

- a. IRGA: 32 T1 Digital Groups
- b. IRGB: 15 TRI-TAC Formatter Digital Groups

### 7.3 SOFTWARE ARCHITECTURE

Software for Digital Network Control (DNC) falls into three categories: development, operational, and maintenance, as shown in Figure 7-43. Operational software consists of programs and data which satisfy the processing requirements of DNC and provide related support functions. Development software is used to generate the operational software and consists of programs such as compilers and editors. Maintenance software is used for off-line checkout of the processors which run the operational software. Development and maintenance software are vendor supplied and are not discussed in this section.

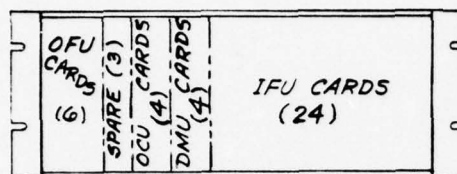
Operational software for DNC can be divided into system sector and nodal level software and DCE Central Control Unit software. Each provides or supports the functions to be performed at a different system control level.

#### 7.3.1 System Control Sector and Nodal Level Software

In order to provide the functions of DNC, software is required at the sector and nodal levels and will run on processors at these levels. The main functions of this software are to provide the man-machine interface and to maintain the data base used to translate between human and machine commands.

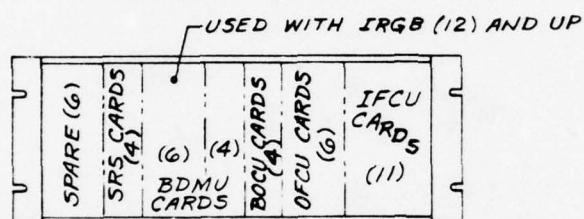
##### 7.3.1.1 Operation

Figure 7-44 shows the components of the DNC software which reside at the sector and nodal levels. Commands from personnel are checked for validity by Command Processing and an appropriate message is returned for commands which are in error. Using information from the data base, valid commands are then translated to DCE Central Control Unit commands and sent to the DCEs for execution. The DCEs

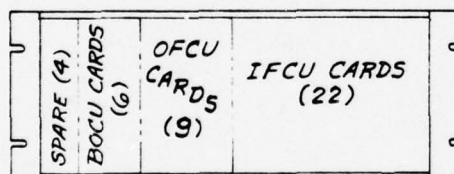


ONE REQD/  
32 T1 DIGITAL GROUPS

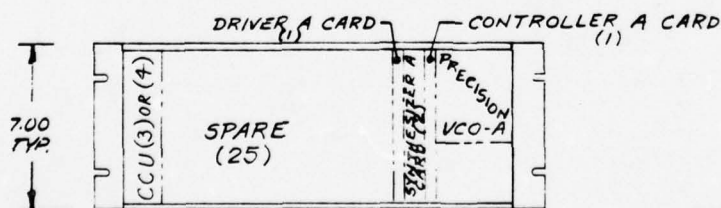
IRGA NEST MODULE



IRGB NEST MODULE A



IRGB NEST MODULE B



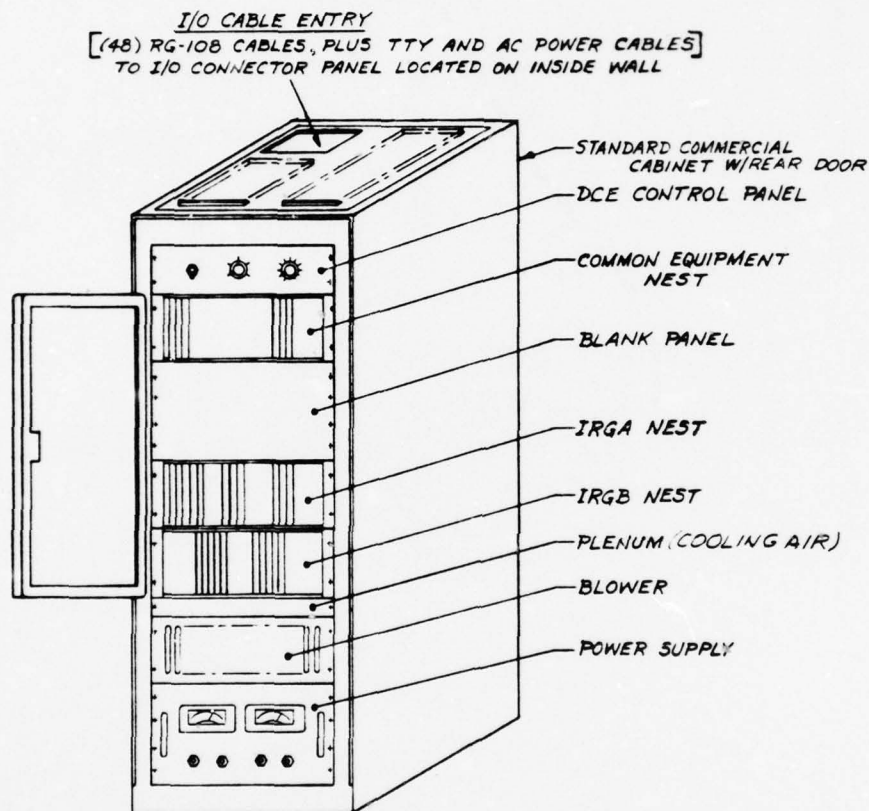
CEG NEST MODULE

NOTE: NEST MAX CAPACITY =  
(41) CARDS @ 0.4" CENTERS

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Figure 7-42A. Nest Modules for DCE Equipment

TYP DCE EQUIPMENT DATA	
CABINET WIDTH	23.09 (IN.)
CABINET HEIGHT	62.00
CABINET DEPTH	24.00
FRONT PANEL WIDTH	19.00
MAX FRONT PANEL HEIGHT	56.00



TYPICAL DCE EQUIPMENT ASSEMBLY  
 [SIZED FOR 32 TI DIGITAL GROUPS (IRGA) AND  
 15 TRI-TAC FORMAT DIGITAL GROUPS (IRGB)]

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Figure 7-42B. Typical DCE Equipment Assembly



AD-A071 672

GTE SYLVANIA INC NEEDHAM HEIGHTS MASS ELECTRONIC SYS--ETC F/G 17/2  
DIGITAL NETWORK CONTROL.(U)  
MAY 77

DCA100-76-C-0064

SBIE -AD-E100 237

NL

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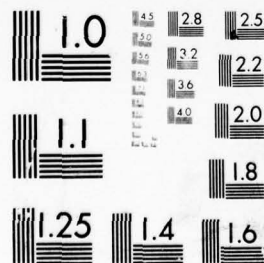
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MICROCOPY RESOLUTION TEST CHART  
NATIONAL BUREAU OF STANDARDS-1963-A

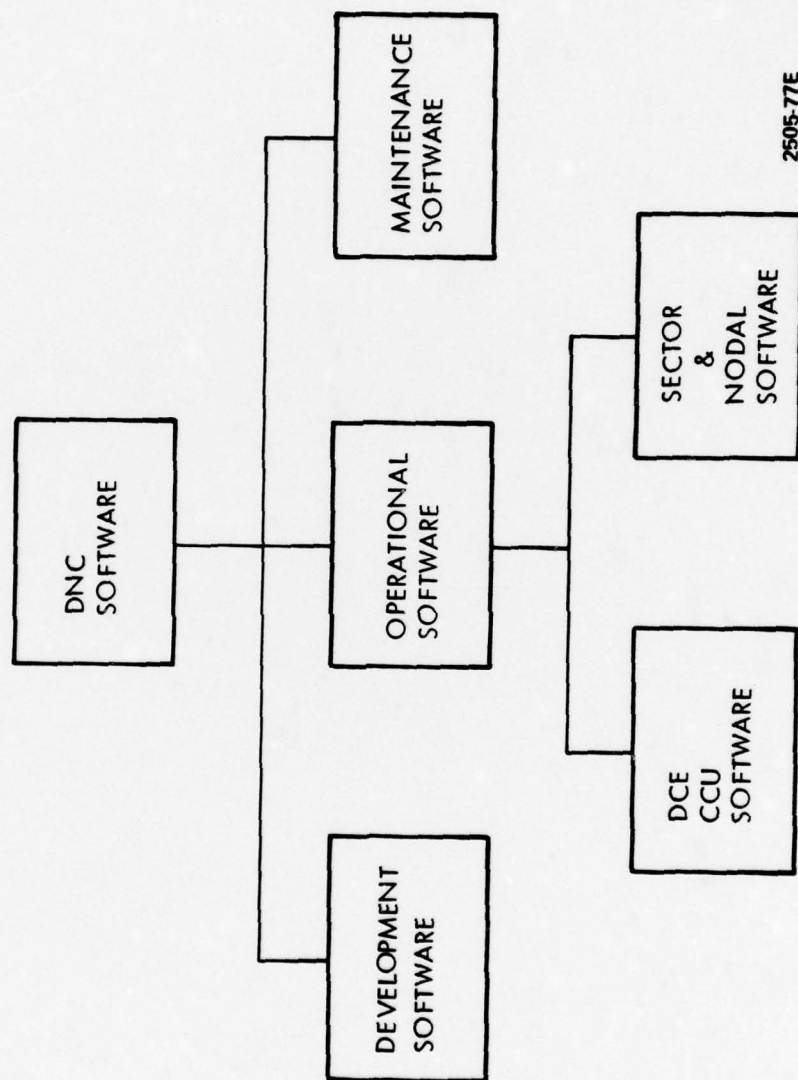
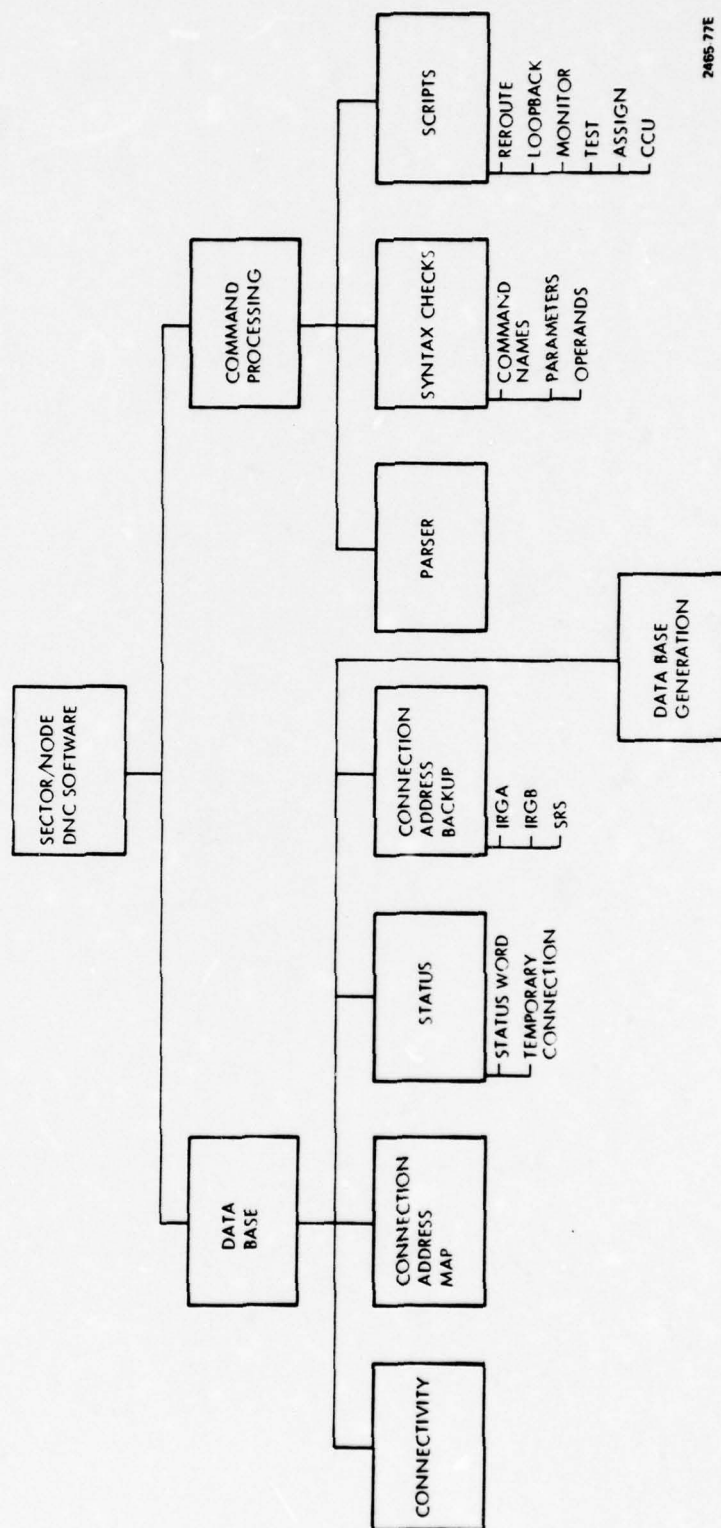


Figure 7-43. Digital Network Control Software



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Figure 7-44. System Control Sector and Nodal Level Software



return status information to the sector/nodal software which examines it and generates a message to the person who originated the command, reflecting the success or failure of the operation. The software updates the data base to reflect the execution of the command. Other data bases in other sectors or nodal areas are updated appropriately, as is the ACOC data base, if required.

One advantage of placing this software at the sector and nodal levels is that it can share programs and data with other software at these levels, such as ATEC. Some of the DNC data base is maintained by ATEC and the DNC software can use this as well as the Data Base Update Programs. Also, the DNC man-machine interface software can use some of the ATEC interface routines, such as TTY or display drivers. If ATEC is not deployed and no other processing capability is placed at the sector and nodal levels instead, then the shared software described above will have to be written in order to support the DNC software described below.

#### 7.3.1.2 Data Base

The data bases at the sector and nodal levels contain the information necessary for the execution of DNC software. This data base contains four types of information needed for DNC: connectivity, mapping of channels to connection addresses, channel status, and connection address backup.

7.3.1.2.1 Connectivity - Associated with each channel is a record containing pertinent information about that channel. It contains the channel name, such as TFELM029801112, in a format which indicates direction (T), site (FEL), link (M0298), supergroup (01), group (1), and channel (12). The record also contains which other channel is connected to the channel, such as RFELM007001624. Note that this example would represent a connection on a thru-group at FEL because it shows a receive (R) channel connected to a transmit (T) channel. This entry must also indicate if the channel terminates at the site. An example is the channel TFELM029801112 indicating that the channel appears as channel 12 on the 1st level multiplexer associated with link M0298, supergroup 01, and group 1. Note that this is identified as a termination by the fact that its direction (T) is the same as the channel to which it connects. An alternative notation would be TFEL0112 which indicates that the channel terminates as the 12th channel on 1st level multiplexer number 01. This is required because the DCE permits channels to terminate on a 1st level multiplexer which is not associated with a link, as would be used for rechannelization. If the channel is connected to the IRGB, the connected-to entry contains the IRGA connection address which connects the channel to the IRGB. Table 7-36 summarizes the portion of the channel record discussed above.

The planned ATEC data base contains the connectivity information for through connections and must be augmented to include terminations as described above if it is to support DNC. Additionally, records similar to these must be maintained for AUTOSEVOCOM II and TRI-TAC channels and subchannels which are connected to the IRGB. If ATEC is not deployed, then a similar data base is required in order to coordinate DNC actions.

TABLE 7-36. CONNECTIVITY ENTRY

TYPE	CHANNEL NAME	CONNECTED TO
Thru-Connection	TFELMØ298Ø1112	RFELMØØ7ØØ1624
Termination	TFELMØ298Ø1112	TFELMØ298Ø1112
Termination - Different Mux Port	TFELMØ298Ø1112	TFELMØ298Ø11Ø4
Termination - Different Mux	TFELMØ298Ø1112	TFELMØ298Ø1312
Termination - Rechannelization	TFELMØ298Ø1112	TFELØ112
IRGB	TFELMØ298Ø1112	16-bit Connection Address

7.3.1.2.2 Connection Address Map - Another entry in each channel record is the connection address associated with the channel. This is a 16-bit number and is an IRGA connection address for 64 kb/s channels, an IRGB connection address for 16 and 32 kb/s AUTOSEVOCOM II and TRI-TAC channels, and a SRS connection address for 2 and 4 kb/s subchannels. This entry is used when translating from human to DCE commands.

The T and R directions of a channel or subchannel will both have the same connection address. Connection addresses are normally assigned at data base generation time, as discussed in Section 7.3.1.2.5.

7.3.1.2.3 Channel Status - The channel status is used by the DNC software to properly execute commands. Figure 7-45 shows the format of the status byte and Figure 7-46 shows the status entry for:

- a. 64 kb/s channels
- b. 16 and 32 kb/s channels
- c. 2 and 4 kb/s subchannels.

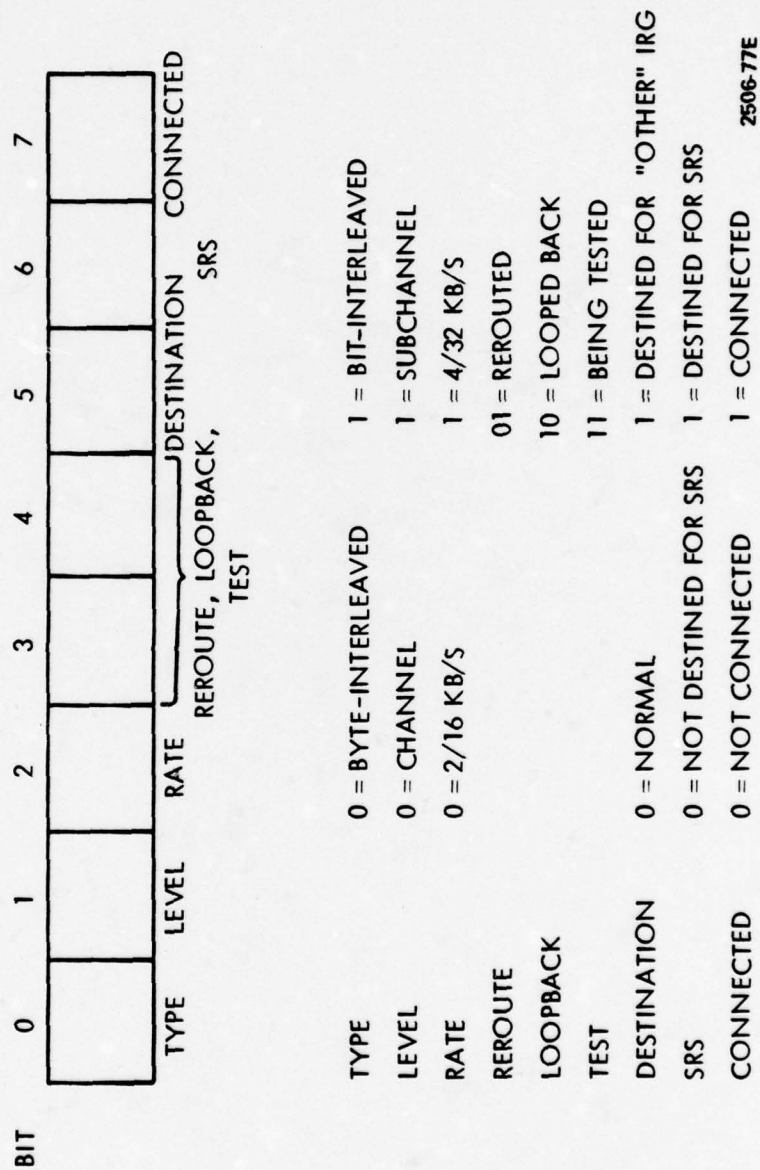
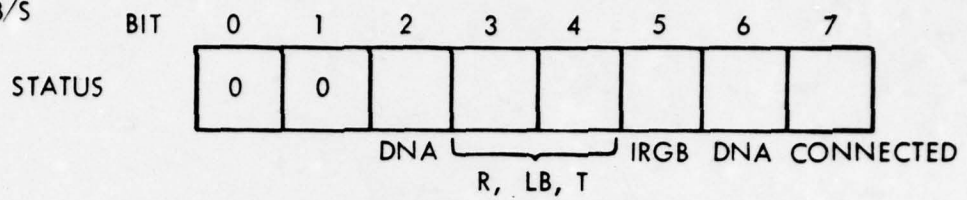


Figure 7-45. Channel Status Byte



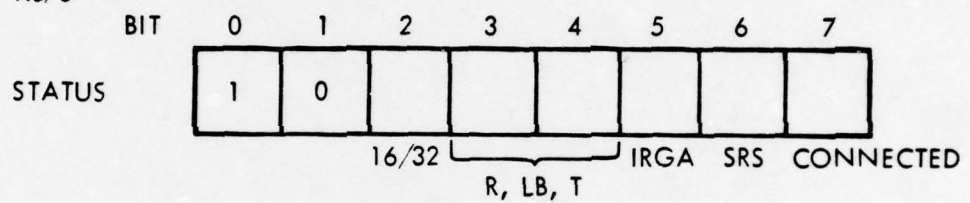
a) 64 KB/S



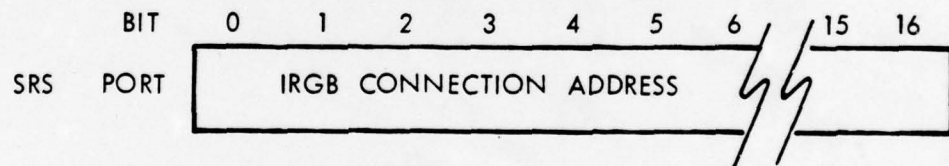
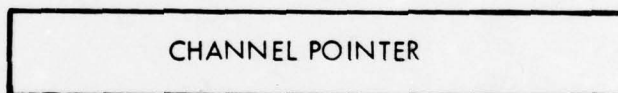
TEMPORARY  
CONNECTED TO



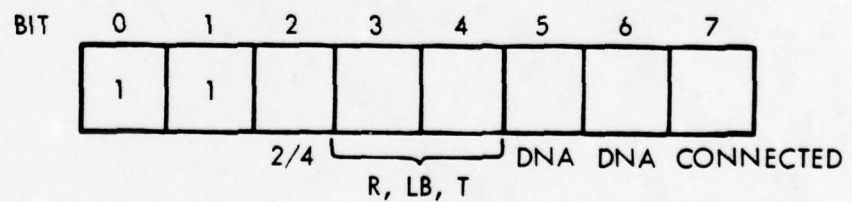
b) 16/32 KB/S



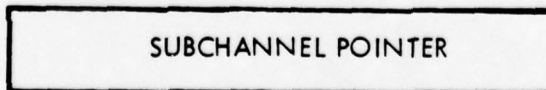
TEMPORARY  
CONNECTED TO



c) 2/4 KB/S



TEMPORARY  
CONNECTED TO



NOTE: DNA = DOES NOT APPLY

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Figure 7-46. Channel Status



The status byte contains pertinent information about each channel or subchannel. The first 3 bits indicate whether it is a 64, 16, or 32 kb/s channel or a 2 or 4 kb/s subchannel. The next two bits indicate if it is currently being rerouted, looped back, or tested. Bit 5 indicates if the channel is connected to the "other" IRG (IRGB for 64 kb/s channels and IRGA for 16 and 32 kb/s channels) and is not used for subchannels. Bit 6 indicates if the channel is connected to the SRS and only applies to 16 and 32 kb/s channels. Bit 7 indicates if the channel or subchannel is currently connected to some other channel.

Each entry also contains a "Temporary Connected To" field. If the channel or subchannel is being rerouted, looped back, tested, or monitored, this field contains a pointer to the channel to which it is temporarily connected. For reroutes it will be some other channel or mux port while for loopback it will be the other direction of the channel. For testing the field will point to a record identifying a piece of test equipment, such as DSG104 (Digital Signal Generator #1, channel 4). Note that when a channel is being rerouted, looped back, or tested its normal connecting channel is disconnected. This is indicated by the "connected" bit in the status word of the connecting channel being cleared to 0. This bit is set when the reroute, loopback, or test is terminated.

An additional field is necessary for 16 and 32 kb/s channels if they are overhead channels which are to be sent to the SRS for subchannel reassignment. This field contains the IRGB connection address which indicates where the channel is connected to the SRS and is normally determined during data base generation.

7.3.1.2.4 Connection Address Backup Tables - The connection address backup tables are copies of the address memories in the DCE IRGA, IRGB, and SRS. Each table contains a header indicating the site, group, and address memory of which it is a copy. An example would be DONA04 which indicates address memory #4 in IRGA at Donnersberg, while DONB01 would indicate address memory #1 in IRGB at Donnersberg. The rest of the table consists of 16 bit connection addresses. An IRGA table contains 768 connection addresses, an IRGB table contains 576 connection addresses, and a SRS table contains 2304 connection addresses. The tables are used for high speed DCE initialization and spare address memory update. These tables could be maintained by the DCE in its own bulk storage if the time to transmit a table to the DCE proves unacceptable. Alternatively, these tables could be eliminated if the time to update a spare memory proves to be unimportant because this data is also maintained in the connection map. This decision depends upon the reliability of the DCE and upon the speed of the communications line between the DCE and the nodal processor.

7.3.1.2.5 Data Base Generation - Associated with the DNC data base is the data base generator. This software routine takes as input the channel connectivity and how the digroups and groups are connected to the DCE, including test equipment, and outputs the data base and the connection address backup tables for the DCE. Further modifications

to the data base prior to bringing up a DCE may be accomplished using data base handling routines. Also required as input is how the IRGA, IRGB, and SRS are interconnected. The data base generator then allocates channels between the IRGA and IRGB and between the IRGB and SRS as needed.

7.3.1.2.6 Data Base Sizing - Table 7-37 presents the size of the data base for three sites. The site descriptions were taken from the DEB IV multiplex plans and estimates of AUTOSEVOCOM II trunk group cross sections. Feldberg is a very large site and is also a switch site. It is planned to have 13 second-level multiplexers and 47 first-level multiplexers. Adenau is planned as an unmanned branching repeater with 6 second-level multiplexers. Giessen is a small terminal site with 1 second-level multiplexer and 3 first-level multiplexers.

TABLE 7-37. DATA BASE SIZE (k bytes)

SITE	CONNECTIVITY	CONNECTION ADDRESS MAP	STATUS	ADDRESS MEMORY BACKUP	TOTAL
FEL	58.7	11.7	29.8	11.9	112.1
ANU	13.4	2.7	6.7	1.5	24.3
GSN	2.9	0.6	1.4	1.5	6.4

The connectivity entry is assumed to be ten bytes long. The first six bytes represent the channel name as follows: byte one is the direction; byte two is the site number (index to a table of site names); byte three is the link number; and bytes four, five, and six represent the supergroup, group, and channel numbers, respectively. The last four bytes form a pointer to the entry representing the "connected-to" channel. Pointers in status entries are also four bytes long.

The data base sizes shown above represent that which is required only for each of the three sites. In other words, if Feldberg is a node with jurisdiction over Adenau and Giessen then the size of the actual data base at Feldberg would be the sum of that for each of the three sites, or 142.8k bytes. This is well within the capabilities of floppy disks and in fact each station could maintain its own section of the data base instead of, or in addition to, the copy at the nodal level. This would be less cost-effective but would facilitate station controller/DCE communication in the event that the DCE is isolated from its nodal processor. This scheme could also be used if no nodal or sector processors as described are deployed; however, some form of DCE coordination must be provided in any event.

#### 7.3.1.3 Command Processing

The Command Processing software accepts and processes commands from personnel or from the DCE. It consists of a parser, a syntax checker, and several execution scripts. When a command is received, the parser is called to return the command name. It is checked to see if it is a valid name and if so the appropriate execution script is performed.

**7.3.1.3.1 Parser** - The parser accepts a character string and returns the first token. A token is a string of non-blank characters surrounded by blanks. For example, if the parser was called with the string "REROUTE~~BA~~~~BB~~~~BB~~" (where "" is a blank), it would return the token "REROUTE" and the new character string "~~BA~~~~BB~~~~BB~~". If called with this new string, it would return the token "A" and the string "~~BB~~~~BB~~". A third call would return "B" and the string "~~BB~~". A fourth call would return an error indicator since there are no tokens in the string.

**7.3.1.3.2 Syntax Checker** - The syntax checker is used to validate the parameters and operands in a command and to convert them to an internal format. It is passed a character string and a set of flags which indicate the legal types of the first token in the string. It returns an internal form of the token, its type, and any error flags which were set during the syntax check. The syntax checker calls the parser to get the first token from the string.

Table 7-38 presents the various token types used in commands to the sector/nodal software. The digroup and PCM channel formats and the test equipment format are as described previously. The formats for AII and TRI-TAC groups, channels, and subchannels are unspecified at this time. However, whatever format is chosen can be accommodated by the syntax checker. The command names are one of the 7 different names as described in Section 7.3.1.3.3. The IRGA, IRGB, SRS" parameter indicates which group the command affects, with three possible values: "A", "B", and "S". "DUPLEX/SIMPLEX" indicates whether the operation applies to one or both directions and "Initiate/Terminate" indicates whether a command is to perform or remove a patch. Connection addresses are represented as three numbers separated by spaces where the first two-digit number refers to the row or column number of a DMU (1 to 6 for IRGA, 1 to 13 for IRGB, and 1 to 2 for SRS), the second two-digit number refers to the group number within a row or column (1 to 32 for IRGA, 1 to 3 for IRGB and SRS), and the last three-digit number refers to the channel bit or byte in the group (1 to 24 for IRGA, 1 to 192 for IRGB, and 1 to 768 for SRS). A column is an OCU and its associated DMUs. The site parameter is a three-letter site code.



TABLE 7-38. TOKEN TYPES

TYPE	EXAMPLE
1.544 Mb/s digroup	TFELMØ298Ø11
64 kb/s channel	TFELMØ298Ø1112
AII/TRI-TAC Trunk Group	?
16/32 kb/s channel	?
2/4 kb/s subchannel	?
Test equipment	DSG1Ø4
Command Name	REROUTE
IRGA, IRGB, SRS	A
DUPLEX/SIMPLEX	DUPLEX
Initiate/Terminate	INITIATE
Connection Address	Ø5Ø4Ø24
Column	Ø5
Site	FEL

After the token is validated and its type determined, it is converted to an internal format. This allows input format changes without requiring extensive software modifications. To change the syntax of an operand or parameter it is only necessary to alter the syntax checker because the rest of the software uses the internal format which remains the same. Note that the internal format may be the same as the input format. Group, channel, subchannel, and test equipment operands are converted to a format which would be compatible with the data base. The "Command Name", "IRGA, IRGB, SRS", and "DUPLEX/SIMPLEX" tokens are converted to binary numbers, as are connection addresses and OCU tokens.

**7.3.1.3.3 Execution Scripts** - After the top level routine calls the syntax checker to validate the command name and convert it to a binary number, it uses this number to select an execution script to perform. Each command has its own execution script which calls the syntax



checker to validate the parameters and operands and then performs the functions of the command. This provides a modular and flexible command structure in which command addition, modification, and deletion involves adding new scripts or changing or deleting old scripts. Table 7-39 shows the 7 commands to the DNC software at the sector and nodal levels. The following sections briefly describe each command. Figure 7-47 summarizes the general command format, the notation used in the command descriptions, and the initial configuration of the connections through the DCE. Note that SI and SO are test or monitoring equipments with SI being a signal sink and SO a signal source, such as a digital signal generator.

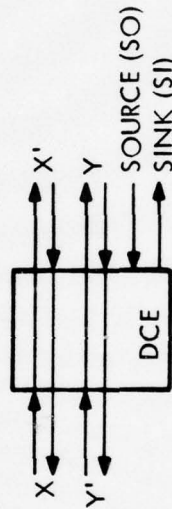
TABLE 7-39. SECTOR/NODAL COMMANDS

NAME	FUNCTION
REROUTE	Temporarily reassign a channel
LOOPBACK	Loopback a channel
MONITOR	Connect a channel to monitoring equipment
TEST	Connect a channel to test equipment
ASSIGN	Reassign a channel on a long term basis
CAML	Down line load a DCE connection address memory
CCU	Send following command to CCU

7.3.1.3.3.1 REROUTE - The format, parameters, and operands of the REROUTE command are shown in Figure 7-48. This command is used to restore a channel temporarily by patching it to another channel. Most of the commands follow the philosophy that the command action should simulate what would happen if the operation had been performed manually using patch cords. This facilitates tech controller training in the use of the DCE. In the example of Figure 7-48, initiating the reroute using the REROUTE command results in the same effect as if a patch cord had been inserted in the jacks for X and Y. That is, X and Y are connected together while X' and Y' are disconnected. Note that X and Y may be groups, channels, or subchannels and the patch may be either for one or both directions.

# COMMAND-NAME PARAMETERS OPERANDS

- COMMAND-NAME: ONE OF 7 COMMAND NAMES
- PARAMETERS: INITIATE - INITIATE AN ACTION (DEFAULT)  
TERMINATE - TERMINATE AN ACTION
- A - COMMAND IS FOR IRGA (DEFAULT)
- B - COMMAND IS FOR IRGB
- S - COMMAND IS FOR SRS
- DUPLEX - BOTH DIRECTIONS
- SIMPLEX - ONE DIRECTION
- UNDERLINED PARAMETERS INDICATE DEFAULTS
- OPERANDS: SUBCHANNELS, CHANNELS, GROUPS, TEST EQUIPMENT, DCE UNITS
- IN FOLLOWING DESCRIPTIONS:
  - [ ] INDICATES PARAMETER CHOICE
  - X, Y, SI, SO ARE OPERANDS
  - INITIAL CONFIGURATION



## ● EXAMPLE COMMANDS

REROUTE INITIATE A FELM029801112 FELM007001624  
REROUTE TERMINATE A FELM029801112

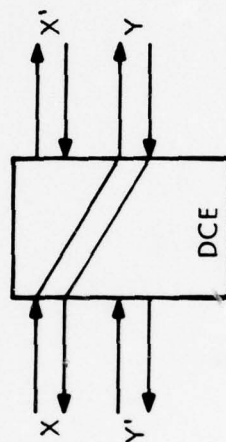
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Figure 7-47. Sector/Nodal NCS Command Format

REROUTE  $\left[ \begin{array}{c} \text{INITIATE} \\ \text{TERMINATE} \end{array} \right] \left[ \begin{array}{c} A \\ B \\ S \end{array} \right] \left[ \begin{array}{c} \text{DUPLEX} \\ \text{SIMPLEX} \end{array} \right] X Y$

● INITIATE

- DISCONNECT X' AND Y'
- CONNECT Y AND Y' TO PREEMPT SIGNAL IF NECESSARY
- CONNECT X AND Y



● TERMINATE

- DISCONNECT X AND Y
- CONNECT X TO X' AND Y TO Y'

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Figure 7-48. Reroute Command

Terminating the reroute would reconnect X to X' and Y to Y', just like the removal of the patch cord. Note also that, after the reroute, if trouble developed in Y and it was desirable to reroute X to Z, the command "REROUTE INITIATE X Z" would connect X to Z and reconnect Y to Y', as would occur if one end of the patch cord has been moved from Y to Z. This is the reason the status entry in the data base indicates if a channel is currently being rerouted so that if another reroute is performed the correct action is taken. The capability is provided to optionally connect users to a preemption signal or message prior to completing the reroute if the user is being preempted.

An additional function of the REROUTE command is necessitated by the fact that the IRGB does not employ double-buffered data memories as is used in the IRGA. When reassigning the bits of a 16 or 32 kb/s channel so that they are contiguous within a T1 frame, the bit order is altered in certain situations. This bit order change is counteracted in the REROUTE execution script by rearranging the connection addresses such that the proper bit order is recovered. Other scripts which reassign channels in the IRGB also have this function.

7.3.1.3.3.2 LOOPBACK - The LOOPBACK command is illustrated in Figure 7-49. As described, it loops back a channel in only one direction and a second loopback command would be required to loopback the other direction. The "DUPLEX/SIMPLEX" parameter is not used in this command because a uni-directional channel cannot be looped back. Note that group loopbacks would simulate a manual patching action at the digital group patch board.

7.3.1.3.3.3 MONITOR - Figure 7-49 also shows the structure of the MONITOR command. This command in effect bridges a channel to bring out one (SIMPLEX parameter) or both (DUPLEX parameter) directions. Subchannels and groups can also be monitored in a similar manner. In the example shown, either X or X' could be monitored because they are connected. If X is rerouted to Y, then the signals monitored at X and X' will be different, since X' is unconnected.

7.3.1.3.3.4 TEST - The TEST command is used to perform off-line tests of a channel, subchannel, or group. In the DUPLEX mode, the receive direction of the channel being tested is connected to a signal sink and the transmit direction is connected to a signal source as shown in Figure 7-50. For a SIMPLEX connection, only one of the above connections is made. As with LOOPBACK and REROUTE X' is disconnected and may be separately tested, looped back, or rerouted.



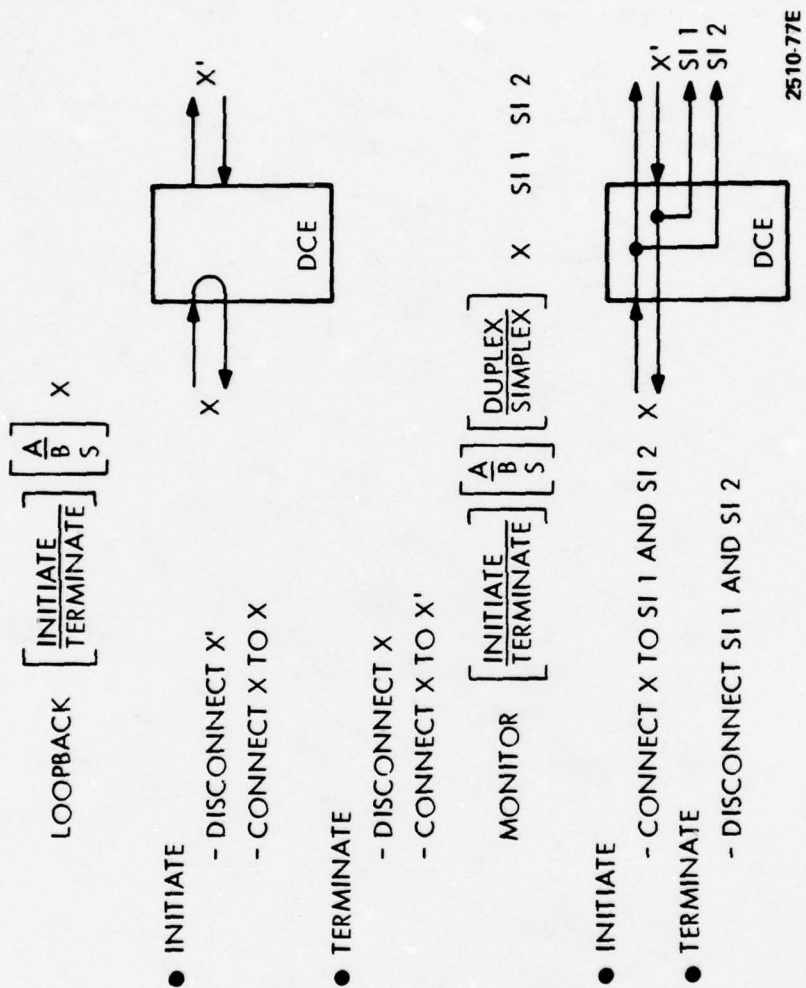


Figure 7-49. Loopback and Monitor Commands

TEST  $\left[ \begin{array}{c} \text{INITIATE} \\ \text{TERMINATE} \end{array} \right] \left[ \begin{array}{c} A \\ B \\ S \end{array} \right] \left[ \begin{array}{c} \text{DUPLEX} \\ \text{SIMPLEX} \end{array} \right] X \text{ SI SO}$

● INITIATE

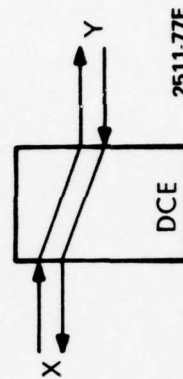
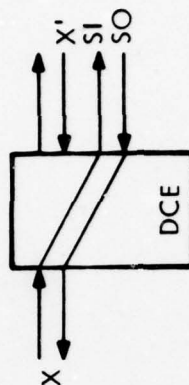
- DISCONNECT X'
- CONNECT X TO SI AND SO

● TERMINATE

- DISCONNECT SI AND SO
- CONNECT X TO X'

ASSIGN  $\left[ \begin{array}{c} A \\ B \\ S \end{array} \right] \left[ \begin{array}{c} \text{DUPLEX} \\ \text{SIMPLEX} \end{array} \right] X \text{ Y}$

● CONNECT X TO Y



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Figure 7-50. Test and Assign Commands

7.3.1.3.3.5 ASSIGN - The ASSIGN command, as shown in Figure 7-50, is different from the previous four commands in that it does not simulate patching actions but rather a long-term wiring change. Its action is similar to the REROUTE command in that it disconnects channels before it creates the new connection. However, it does not reconnect channels if it is used to restore the old connectivity. It modifies the "connected to" field in the status entry while REROUTE modifies the "temp connected to" field. For example, after execution of "ASSIGN A X Y", the connectivity would be as in Figure 7-48 for REROUTE. If "ASSIGN A X X'" was then executed, X would be connected to X' as with REROUTE, but now both Y and Y' are unconnected. Similarly, if the sequence "ASSIGN A X Y, ASSIGN A X Z" was executed, again Y and Y' would be unconnected. The INITIATE/TERMINATE parameter is not used with the ASSIGN command.

7.3.1.3.3.6 Connection Address Memory Load (CAML) - The CAML command is used to down-line load the address memories of a DCE. In it is specified the address memory (column number) to update the DCE module which contains the indicated address memory (A, B, or S), and the site at which the DCE is located. This command is issued to the NCS by the DCE during initialization of the address memories and during fault correction to update the spare OCU prior to switching it on-line. The script for this command uses the connection address backup tables in order to provide high speed transfer of connection addresses to the DCE. Note that if a second CAML command is received from a DCE for which a CAML command is already in progress, the first command is aborted.

7.3.1.3.3.7 CCU - The CCU command is used to send commands directly to the DCE. The site of the target DCE is specified along with the CCU command, as described in Section 7.3.2.5.1. Operands of the CCU command, such as connection addresses, are input in the format described previously and are translated to the internal formats by the sector/nodal software prior to transmission to the DCE. This reduces the amount of bits transmitted to the DCE.

7.3.1.3.4 Supporting Routines - Several other programs and routines are necessary for the functioning of the DNC sector/nodal software. An operating system is required to run the DNC software and interface it to the outside world. Keyboard and display driver routines interface the software with sector and nodal controllers while telecommunications programs handle transmission protocols to allow the DNC software to communicate with station controllers, DCEs, and the ACOC (if necessary). Programs are also needed to manage the data base in order to access, update, add, and delete entries. These data base programs are also used by the data base generator, as described in Section 7.3.1.2.5.

7.3.1.3.5 Responses - Responses are generated by the sector/nodal software to the controller to indicate the success or failure of a command. Error messages include syntax errors, semantic errors, execution errors, and software errors. Informative messages reflect conditions other than errors such as successful completion. Table 7-40 presents examples of these responses.

TABLE 7-40. RESPONSES

Syntax Error Message: 01 SYNTAX ERROR - TOO FEW OPERANDS
Semantic Error Message: 12 OPERAND "ABCD" NOT IN DATA BASE
Execution Error Message: 13 DCE FAULT - COMMAND ABORTED
Software Error Message: 26 SOFTWARE ERROR: SYNTAX CHECKER FAULT
Informative Message 01 COMMAND COMPLETED

7.3.1.3.6 Sizing - Estimates of the size of the command processing software indicate that it will require roughly 5000 bytes of memory. This estimate is based on the Intel 8080 microprocessor instruction set (as used in the CCU) and would be different for different microprocessors or minicomputers. This estimate does not include the supporting software described above.



### 7.3.2. DCE Central Control Unit Software

The DCE Central Control Unit (CCU) is the interface between the DCE hardware and the sector/nodal software and human personnel. It also provides housekeeping functions and fault detection, isolation, and correction control for faults within the DCE. It utilizes an Intel 8080A microprocessor, as described in 7.2.2.3.1, to execute the software. Peripheral Interface Adapters (PIA) and Universal Synchronous/Asynchronous Receiver/Transmitters (USART), also discussed in Section 7.2.2.3.1, interface the CCU to the hardware and system control communication equipment. Figure 7-51 shows the various elements of the CCU Software.

#### 7.3.2.1 Operation

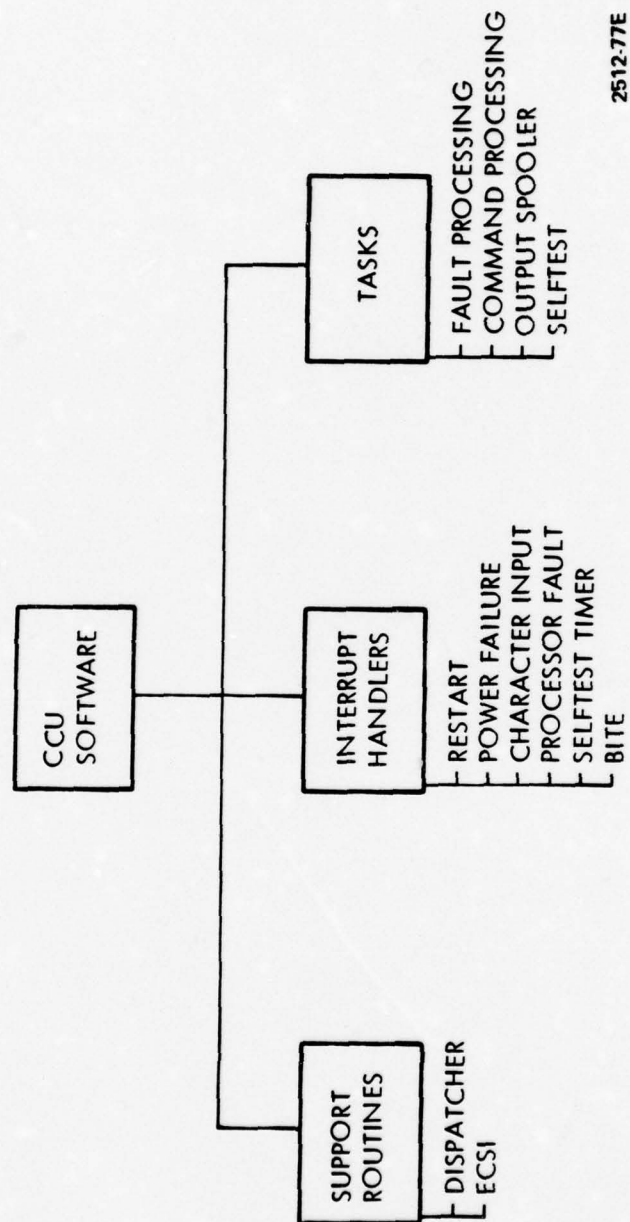
The CCU software consists of six interrupt routines, four tasks, and two support functions, as shown in Figure 7-51. Interrupt routines handle information coming in from the hardware and system control and call the dispatcher to activate the appropriate task. Tasks are executed on a priority basis and can be preempted by higher priority tasks. Some tasks have queues of work to perform while others do not. The Equipment Control and Status Interface (ECSI) routine interfaces the software to the PIAs and helps to prevent software changes from requiring hardware modifications and vice versa.

Several tables are used by the CCU software in performing its tasks. The Hardware Status Table contains information on what cards are in the system and which cards have been flagged as faulty. This table is used by the fault isolation software. The Initialization Table is used to set up the IFCU selectors and group multiplexers upon DCE start-up. Both tables are loaded locally when the DCE is initialized or can be down-line loaded from the NCS.

#### 7.3.2.2 Support Routines

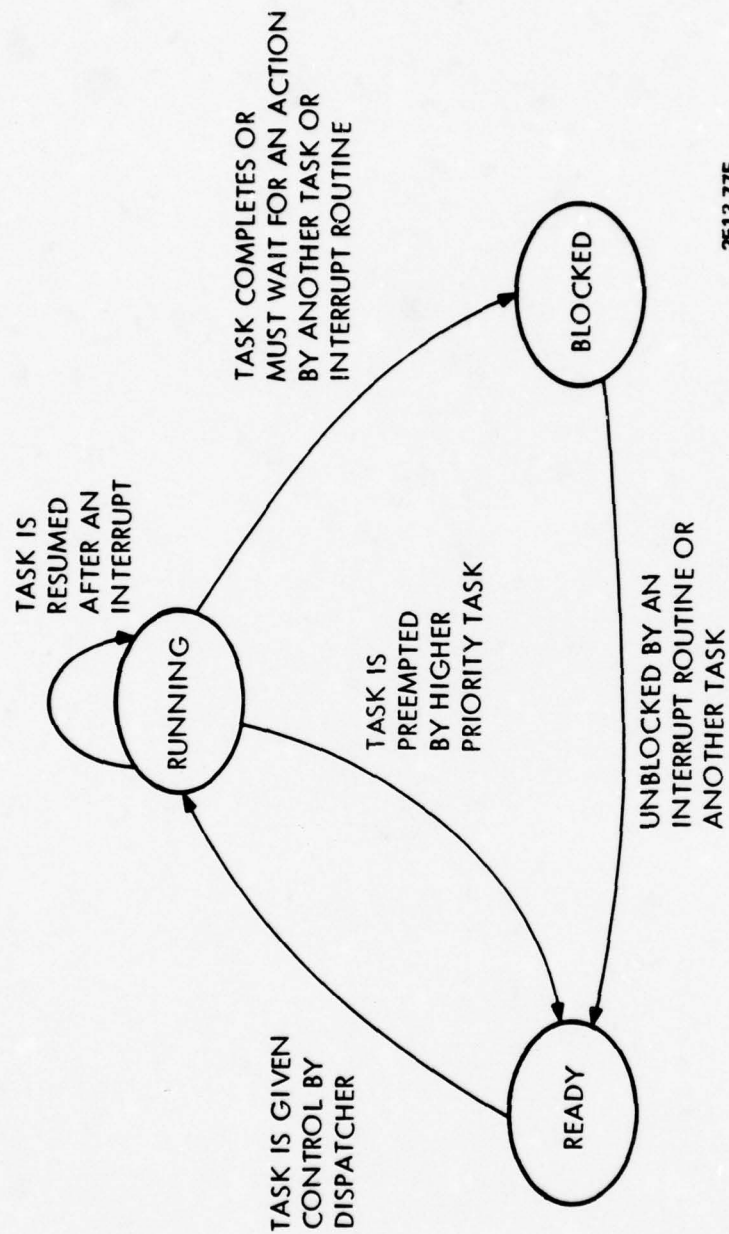
The support routines provide the framework in which the tasks and interrupt routines perform their functions. These two routines plus certain interrupt routines and the output spooler task form an executive for the CCU.

7.3.2.2.1 Dispatcher - The dispatcher controls the execution of the four tasks. Control is passed to it by the interrupt routines and tasks upon completion of execution. When the dispatcher gets control, it checks to see if any tasks are running or ready to run and selects the highest priority task for execution. If this task is currently running, execution is resumed where it left off. If the task is not running but ready, the running task is preempted in order to execute the higher priority task. Tasks are blocked when they have nothing to do or are waiting for some action to occur. Figure 7-52 illustrates the different states of a task.



2512-77E

Figure 7-51. CCU Software



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Figure 7-52. Task Execution States



Task blocking is controlled by lock bits which can be set to indicate that the task is blocked or can be cleared to unblock a task. Each task has one lock bit to indicate task completion and may have more lock bits for synchronization purposes. For example, if a task needed to wait for an interrupt to occur, it would set its lock bit associated with this interrupt and transfer control to the dispatcher. This task is now blocked and will not be given control by the dispatcher. When the interrupt occurs, the interrupt routine will clear the lock bit and transfer control to the dispatcher. Now the task is unblocked and ready to run. One problem with this scheme is that a deadlock can occur when two tasks are blocked, each waiting for the other. This is not a problem in a system as small as the CCU software because it is feasible to check for all possible deadlock conditions among the four tasks and modify the design as appropriate.

Each task also has an "active" bit which indicates if the task is running or not. If the dispatcher finds a tie for the highest priority between two tasks, the one that is active will be given control. If neither is running an arbitrary decision is made. Each task also has a register save area to keep track of where it is in its execution.

7.3.2.2.2 Equipment Control and Status Interface - The ECSI routine provides an interface between the CCU software and the PIAs. It accepts commands from the tasks to send or receive information via the PIAs and translates these to appropriate hardware commands. It monitors the success or failure of a hardware command and can unblock the fault isolation task in the event that a failure occurs. It also modifies hardware commands to reflect the substitution of the spare column in the DCE. Commands destined for faulty units which have been replaced temporarily by the spare must be redirected to the spare column. The ECSI also generates the necessary parity bits for the hardware commands and checks the parity on status words coming from the hardware.

#### 7.3.2.3 Interrupt Routines

The interrupt routines provide another link between the hardware of the DCE and the CCU software. When an interrupt occurs the running task is halted and control is given to the proper interrupt routine. When it completes it transfers control to the dispatcher, as discussed in Section 7.3.2.2.1. Each interrupt has a priority which is used in two ways. The Priority Interrupt Controller (PIC) uses the priorities to break ties when two interrupts arrive simultaneously. The PIC also masks lower priority interrupts which helps to avoid system confusion when multiple interrupts occur. Note that the priority is not a measure of importance but indicates which interrupts require more rapid acknowledgement and processing.



When an interrupt occurs the PIC interrupts the 8080A CPU and places a RESET instruction onto the data bus which contains the address of the start of the appropriate interrupt routine. The RESET instruction causes the CPU to save the program counter (location of the next instruction to be executed) and branch to the specified location, thus giving control to the interrupt routine.

**7.3.2.3.1 Restart** - The restart interrupt is used to initialize the processor and peripheral control chips. It is assigned priority 0 (highest priority) as is standard on the 8080. This routine checks to see if the restart was caused by a power up or by pressing the restart button. If a power up, it initializes the PIAs, USARTs, and the IFCU and issues the CAML command to load the address memories (refer to Section 7.3.1.3.6). It loads the registers from the power failure register save area and continues execution. If the restart button is pressed, all registers and RAM are cleared followed by initialization of the PIAs and USARTs. The routine requests that the system tables be loaded either manually or from the nodal level software. It then initializes the IFCU and branches to the dispatcher to begin execution.

**7.3.2.3.2 Power Failure** - The power failure interrupt has priority 1 and occurs when the power supply fails. There is a small amount of time between the detection of the failure and the loss of logic operability. During this time the registers are saved in the power fail save area in RAM which is backed up by batteries. When the power returns a restart is performed, as described in Section 7.3.2.3.1. Note that when the DCE is first powered up the RAM will contain random bits, so the restart button must be pressed to initialize the memory.

**7.3.2.3.3 Character Input** - The character input interrupt is raised whenever a character is received by one of the USARTs for input to the software. The routine performs the ACK-NAK protocol (or other protocol if required) and groups the characters together to form a string representing a command. When a complete command is formed it is placed in the command queue and the command processing task is unblocked. Note that commands may be coming from several locations simultaneously (nodal processor, station controller, and local teletype) and the character input routine must keep the characters separate. This interrupt has priority 2.

**7.3.2.3.4 Processor Fault** - This interrupt occurs when the hardware detects a parity error on the output of a PIA. This could indicate either a faulty PIA or 8080 processor. The hardware isolates the PIA from the switching matrix so that bad commands will not cause misrouting of data. The processor fault routine attempts to issue a message indicating the problem and also may run diagnostics. The processor fault interrupt has priority 3.

**7.3.2.3.5 Selftest Timer** - This interrupt occurs when the timer set by the selftest task times out. The routine unblocks the selftest task and branches to the dispatcher. The priority of this interrupt is 4.

7.3.2.3.6 BITE - When the DCE Built-In Test Equipment (BITE) detects a fault, it raises the BITE interrupt. The interrupt routine unblocks the fault processing task and branches to the dispatcher. This interrupt has priority 5, the lowest of the six interrupts.

#### 7.3.2.4 Tasks

The four tasks are the heart of the CCU software. They perform the functions necessary to reassign channels and isolate faults and interact with the support and interrupt routines and with each other.

7.3.2.4.1 Fault Processing - The fault processing task performs fault isolation for the DCE units and initiates corrective actions. It is unblocked by the BITE interrupt routine or by the selftest task. It has the highest priority of the four tasks and runs with the BITE interrupt disabled.

When the task gets control it first determines which BITE indicator(s) triggered the interrupt. It clears the affected status buffers to check if the fault is transient. If the fault does not reoccur it is transient and recorded in the transient fault log. Otherwise, it is a hard fault. Using the status buffer contents and the hardware configuration table, the task isolates a hard fault to as low a level as possible, with the lowest level being a card. If it is a DMU or an OCU card and the spare is available, it is switched in for the column containing the faulty unit. The faulty unit is flagged as such in the hardware configuration table and a message is sent to the station controller indicating the fault and the faulty card. For those faults which cannot be isolated to the card level but can be isolated to a column the spare is switched in, if available, and the controller is informed. For other faults only a message is sent to the controller. The task also clears the status buffers and sets a flip-flop which prevents the fault from causing another interrupt.

7.3.2.4.2 Command Processing - The command processing task is similar to the sector/nodal command processing software, as described in Section 7.3.1.3. It also consists of a parser, syntax checker, and execution scripts and operates in an identical manner. The parameters and operands are the same as for sector/nodal commands and the command formats, shown in Figure 7-53, illustrate the types of legal parameters and operands used in CCU commands.

7.3.2.4.2.1 Write Connection Address - The WCA command is used to modify the connection address memories of a DCE. It causes the connection address specified by the first operand to be written into the address memory location specified by the second operand. The parameters and operands are first checked for proper syntax and semantics. In this case semantics refers to whether or not the connection addresses exist. The ECSI is then passed the command which

WCA  $\begin{bmatrix} A \\ B \\ S \end{bmatrix}$  CA CA

RCA  $\begin{bmatrix} A \\ B \\ S \end{bmatrix}$  CA

RER  $\begin{bmatrix} A \\ B \\ S \end{bmatrix}$  COLUMN

RSB  $\begin{bmatrix} A \\ B \\ S \end{bmatrix}$  COLUMN

CHECK  $\begin{bmatrix} A \\ B \\ S \end{bmatrix}$  COLUMN

BACKUP  $\begin{bmatrix} \text{INITIATE} \\ \text{TERMINATE} \end{bmatrix}$   $\begin{bmatrix} A \\ B \\ S \end{bmatrix}$  COLUMN

LOAD  $\begin{bmatrix} A \\ B \\ S \\ \text{ALL} \end{bmatrix}$   $\begin{bmatrix} \text{UNITS \#} \\ \text{ALL} \end{bmatrix}$

TRANSIENT

SELFTTEST

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Figure 7-53. CCU Command Formats



translates it to a five-byte WCA hardware command to be executed by the appropriate OCU. A message is returned to the controller indicating the success or failure of the command. This script also accepts WCA commands from the nodal software in the five-byte internal format. Using this format between the nodal software and the DCE reduces the number of characters which must be transmitted. Most of the sector/nodal commands result in WCA commands being sent to the DCE.

7.3.2.4.2.2 Read Connection Address - The RCA command is similar to the WCA command except that a connection address is read from the specified address memory location. The command is used to check the functioning of address memories. It has a five-byte format similar to the WCA command and can be issued in this form from the nodal software. It is used mostly by sector/nodal and CCU software but is provided for use by the controller for completeness.

7.3.2.4.2.3 Reset Error - The RER command clears the status buffer of the OCU in the specified column. It is used in its five-byte hardware command form to check for transient faults and to clear status buffers after a fault is isolated and corrected. It is provided as a human interface command for completeness.

7.3.2.4.2.4 Read Status Buffer - The RSB command is used in conjunction with the RER command in fault isolation. There is no corresponding hardware command for the RSB command because the processor reads the status buffers via the PIAs and only requires minimal assistance from the OCU. The command is used mainly between the fault isolation task and the ECSI.

7.3.2.4.2.5 SELFTEST - The SELFTEST command causes the selftest task to be unblocked. It is used when bringing up a DCE to check out the hardware and when a DCE is reconfigured (e.g., adding an OCU and DMUs or adding an IRGB to the existing IRGA). Refer to Section 7.3.2.4.4 for a description of the selftest task.

7.3.2.4.2.6 CHECK - The CHECK command performs a selftest check on a specific unit as opposed to the entire DCE. This can be used by maintenance personnel using "shotgunning" to isolate faults which were not isolated by the DCE. The SELFTEST command obviously could also be used but requires more time. Most of the time spent performing a check is in the transmission of connection addresses from the nodal software to update the spare address memory. SELFTEST would update the spare once for each address memory while CHECK only updates it for the address memory to be tested. Both the SELFTEST and CHECK commands update the hardware configuration table to reflect failed and repaired units.



7.3.2.4.2.7 BACKUP - The BACKUP command provides manual control of the spare column. It is used to switch-in the spare column when a fault is isolated manually and also to change for which column the spare is substituted. For example, if a fault occurs and is isolated by the DCE to a certain OCU, the spare will be automatically switched in. If a second failure then occurs in a different OCU and this OCU handles more high priority traffic, the BACKUP command could be used to restore service to the higher priority traffic. The BACKUP command is also useful during manual fault isolation.

7.3.2.4.2.8 LOAD - The LOAD command causes the CCU to issue one or more CAML commands to the nodal software (refer to Section 7.3.1.3.3.6) to update connection address memories. The LOAD ALL ALL command is used when the DCE is first brought up. During operation the LOAD command can be used for manual fault isolation and to initialize newly added address memories during expansion.

7.3.2.4.2.9 TRANSIENT - The TRANSIENT command causes the CCU to print out the transient fault log. This aids maintenance personnel in the detection of intermittent faults and potential hard fault conditions which cause abnormal numbers of transient faults. The command also clears the transient fault log after it is printed.

7.3.2.4.3 Output Spooler - The output spooler is the counterpart of the character input interrupt routine. Other tasks and support routines place messages in the output spooler's queue for it to transmit to the station controller or to the nodal software. Using a spooler prevents messages from being printed in the middle of another message. For example, if the command processing task is printing a response to the controller and a fault occurs, printing will cease while the higher priority task executes. If the fault processing task prints a message, it will appear somewhere in the middle of the message from the command processing task. With the spooler the fault processing message will not be printed until the printing of the first message is completed.

Messages from the CCU are similar to those from the sector/nodal software. In addition, there are special status messages sent from the CCU to the NCS in response to WCA, RCA, and RSB commands. Like the short five-byte version of the commands, this short message reduces the load imposed by the DCE on the system control communications facilities. Sample messages are shown in Table 7-41.

TABLE 7-41. EXAMPLE MESSAGES FROM CCU

02	SYNTAX ERROR - ILLEGAL COMMAND NAME
27	ERROR - IRGB NOT IMPLEMENTED
13	DCE FAULT - COMMAND ABORTED
26	SOFTWARE ERROR - UNKNOWN REQUEST TO ECSI
01	COMMAND COMPLETED
119	SPARE IMPLEMENTED IN IRGA FOR UNIT 2
113	DMCP - IRGB DMU6 FAULTY
128	CHECK - UNIT 3 OK
127	SELFTEST - IRGA UNIT 1 FAILED VERIFY TEST

7.3.2.4.4 Selftest - The selftest task performs a check on hardware faults which would not be detected by the BITE and also checks the BITE itself. The verification test, TEST hardware command, and intentionally illegal hardware commands are used to exercise the system.

The verification command is used to detect faults which cannot be detected by the BITE. The spare column must be available to perform this test. The spare address memory is updated to match that of the OCU in the column to be checked by issuing the appropriate CAML command to the nodal software. After the spare is updated the outputs of the spare column and the column being tested should be identical, allowing for a 500  $\mu$ sec start-up transient. If the outputs differ, either the spare column or the tested column has a fault. Updating the spare and comparing it with another column provides more information. If this test fails, either both tested columns were faulty or, more likely, the spare is faulty. The third possibility, that both comparison circuits failed is also less likely than a single failure.

The selftest task tests each column in the IRGA, IRGB, and also tests the SRS. A test failure in the SRS cannot be isolated, as described above, because there are only two columns (i.e., one on-line and one spare column). The CHECK command uses this test but only on a specified column.

The TEST hardware command (not to be confused with the TEST sector/nodal command) induces errors into the hardware. During BITE checkout the BITE interrupt is disabled. The TEST command causes the hardware to inject parity errors into the DMU/OCU data busses and the

CCU/OCU command bus. If Data Memory Parity Check (DMPC) faults and Command Parity Check (CPC) faults do not occur for all DMUs and OCUs then a parity checker circuit has failed and appropriate action is taken, as in the fault processing task. CHECK also uses this test.

The third part of the selftest task issues a WCA command to an OCU with a bad parity bit in the connection address. A Connection Address Parity Check (CAPC) should be returned. If not, the parity checker is faulty. Also, if a CAPC is returned, the WCA command should not have been executed. By doing an RCA command, the selftest task can check whether or not the WCA command was inhibited. If not, the inhibit circuitry has failed.

Selftest also runs diagnostics on the 8080 processor and memory to check for CCU faults. These tests exercise the processor and checkout the registers and busses for faults such as bits stuck at zero or one. The RAM is also checked for problems. If a fault is discovered, the CCU activates the processor lockout and issues a message to the station controller.

#### 7.3.2.5 Size

Table 7-42 presents the size estimates for the CCU software. The estimates were based on the 8080A microprocessor and would be similar for other microprocessors.

TABLE 7-42. CCU SOFTWARE SIZE (K BYTES)

Dispatcher	0.1
ECSI	1.0
Interrupt Routines	0.5
Fault Processing Task	1.0
Command Processing Task	2.0
Output Spooler	0.2
Selftest Task	1.0
Miscellaneous (Diagnostics)	<u>2.0</u>
Total ROM	<u>7.8k bytes</u>
Total RAM	2.0k bytes
(System tables, queues, buffers, etc.)	



### 7.3.2.6 Timing

Table 7-43 presents the timing estimates for a successfully executed REROUTE command. Nodal Control Subsystem (NCS) cpu time includes processing of the REROUTE command, generation of commands to the DCE, examination of the status returned from the DCE, and response generation to the originator of the REROUTE command. An average instruction execution time of  $1\mu$  sec is assumed. DCE CCU cpu time includes processing of the command from the NCS, generation of hardware commands, examination of the status returned from the hardware, and status message generation to the NCS. The average instruction execution time assumed here is  $5\mu$  sec. Data base access time is estimated by determining the number of random accesses to disk and using an average random access time of 50 msec. Two figures are shown for the transmission time of information between the NCS and the DCE. These include both the time to send the commands to the DCE and the time to send the status to the NCS. It can be seen that at 150 baud the transmission time dominates while for 2400 baud the data base access time dominates.

Table 7-44 shows the times for a down-line load of one DCE IRGA connection address memory (768 connection addresses) from the NCS for two different rates. This operation consists of the transmission of some introductory information to the DCE followed by 768 WCA commands. After this is completed, the DCE returns a status message indicating a successful operation. Since NCS and DCE cpu time proceeds in parallel with the transmission of commands, it is not included. Also, few random accesses to the disk are necessary because the connection addresses are stored sequentially in the Connection Address Backup Table allowing high speed accessing. Therefore this time is not included in the estimate.

TABLE 7-43. REROUTE COMMAND TIMING

NCS CPU Time	0.6 msec
DCE CCU CPU Time	1.5 msec
NCS Data Base Access Time	500.0 msec
NCS-DCE Transmission Time	
150 baud	1700.0 msec
2400 baud	110.0 msec
Total Time 150 baud	2202.1 msec
2400 baud	612.2 msec

TABLE 7-44. IRGA ADDRESS MEMORY LOAD TIMING

NCS-DCE Transmission Time	
150 baud	12.0 min.
2400 baud	0.75 min.



#### 7.4 RELIABILITY/AVAILABILITY/MAINTAINABILITY (RAM)

In Section 4.6, a channel availability requirement for the DCE was established. In this section, the basic hardware and software architectures of the DCE as conceptually designed in Sections 7.2 and 7.3 are examined with respect to their ability to satisfy this requirement. The relationship between equipment redundancy and DCE reliability is discussed and the degree of hardware redundancy required is determined.

The RAM analysis of the DCE consists of a part count reliability prediction and construction of functional block diagrams. Math models are developed and quantified using estimated failure rates and restoral times to derive overall reliability/availability prediction results. Additionally, a preliminary maintenance concept is established to define organizational level, intermediate level, and depot level maintenance requirements.

##### 7.4.1 Component Reliability Predictions

Reliability predictions are made using MIL-HDBK-217B, Section 3. The predictions are based upon the hardware design and associated card partitioning, corresponding math models, and a piece part reliability analysis. A ground fixed environment is assumed.

Results of the card reliability analysis are shown in Tables 7-45 and 7-46 for the IRGA and IRGB, respectively. The CEG analysis including vendor supplied power supply failure rates is shown in Table 7-47. The information in these tables provides a basis for determining DCE reliability and availability. It is assumed that miscellaneous DCE mechanical and electrical hardware such as connectors, harnesses, and panel controls play an insignificant role in DCE availability and are therefore neglected in this analysis.

For convenience of calculation, the failure rates of some of the components were combined. Specifically, the following elements are considered collectively:

- a. The SDMU and SOCU
- b. The BDMU and BOCU
- c. The MTU card oscillator subassembly.

##### 7.4.2 Basic DCE Reliability

A reliability model was constructed to represent each of the three DCE equipment groups and its card/module functions. Figures 7-54 through 7-56 illustrate the model configured to handle a 16 kb/s channel. In these figures, parallel paths denote redundant elements in a 1 for N hot standby configuration, where N is given by the total number of in-service elements in the parallel paths. As discussed in Section 6.3.3.2, the CCU includes a lockout capability which prevents improper connections in the event of a failure; therefore, the CCU is not a consideration in the channel reliability analysis.

TABLE 7-45. INTERFACE AND REASSIGNMENT  
GROUP A (IRGA) CARD FAILURE RATES\*

NO.	CARD	FAILURE RATE X $10^{-6}$ (1/HR.)	FAILURE RATE SOURCE
	DESCRIPTION		
1.	IFU Framing Unit Card	31.97 ( $\lambda_{A1}$ )	MIL-HDBK-217B Section 3
2.	IFU Digroup Buffer Card	29.87 ( $\lambda_{A2}$ )	MIL-HDBK-217B Section 3
3.	IFU Frame Alignment Card	39.31 ( $\lambda_{A3}$ )	MIL-HDBK-217B Section 3
4.	IFU Channel Selector Card	1.67 ( $\lambda_{A4}$ )	MIL-HDBK-217B Section 3
5.	DMU Card	13.62 ( $\lambda_{A5}$ )	MIL-HDBK-217B Section 3
6.	AOCU Controller Card	11.18 ( $\lambda_{A6}$ )	MIL-HDBK-217B Section 3
7.	AOCU Address Memory Card	3.77 ( $\lambda_{A7}$ )	MIL-HDBK-217B Section 3
8.	OFU Card No. 1	4.30 ( $\lambda_{A8}$ )	MIL-HDBK-217B Section 3
9.	OFU Card No. 2	1.16 ( $\lambda_{A9}$ )	MIL-HDBK-217B Section 3
10.	OFU Card No. 3	11.33 ( $\lambda_{A10}$ )	MIL-HDBK-217B Section 3

\*Assuming B-2 Quality Level

TABLE 7-46. INTERFACE AND REASSIGNMENT  
GROUP B (IRGB) CARD FAILURE RATES\*

NO.	CARD DESCRIPTION	FAILURE RATE X $10^{-6}$ (1/HR.)	FAILURE RATE SOURCE
1.	IFCU Framing Unit Card	31.97 ( $\lambda_{B1}$ )	MIL-HDBK-217B Section 3
2.	IFCU Digroup Buffer Card	29.87 ( $\lambda_{B2}$ )	MIL-HDBK-217B Section 3
3.	IFCU Frame Alignment Card	21.04 ( $\lambda_{B3}$ )	MIL-HDBK-217B Section 3
4.	IFCU Multiplexer and Conversion Card	18.76 ( $\lambda_{B4}$ )	MIL-HDBK-217B Section 3
5.	IFCU Multiplexer Control Card	18.60 ( $\lambda_{B5}$ )	MIL-HDBK-217B Section 3
6.	BDMU Card	} 83.65 ( $\lambda_{BD}$ )	MIL-HDBK-217B Section 3
7.	BOCU Card		MIL-HDBK-217B Section 3
8.	SDMU Card	} 95.42 ( $\lambda_{BS}$ )	MIL-HDBK-217B Section 3
9.	SOCU Card		MIL-HDBK-217B Section 3
10.	OFCU Card No. 1	5.3 ( $\lambda_{B10}$ )	MIL-HDBK-217B Section 3
11.	OFCU Card No. 2	19.22 ( $\lambda_{B11}$ )	MIL-HDBK-217B Section 3
12.	OFCU Card No. 3	16.62 ( $\lambda_{B12}$ )	MIL-HDBK-217B Section 3
13.	OFCU Card No. 4	18.60 ( $\lambda_{B13}$ )	MIL-HDBK-217B Section 3

\*Assuming B-2 Quality Level

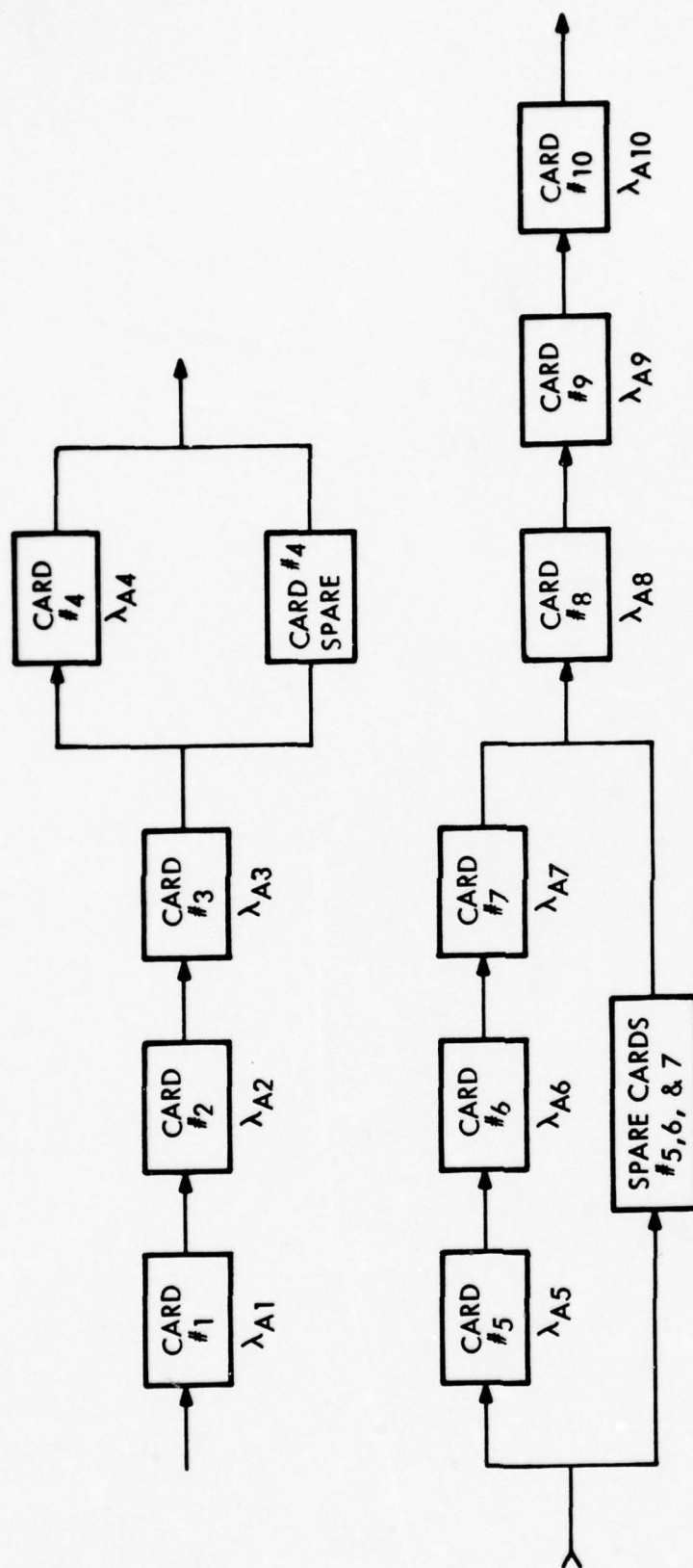


TABLE 7-47. COMMON EQUIPMENT GROUP (CEG) FAILURE RATES\*

NO.	DESCRIPTION	FAILURE RATE X $10^{-6}$ (1/HR.)	FAILURE RATE SOURCE
1.	Power Supply #1	20.00 ( $\lambda_{C1}$ )	Vendor Supplied
2.	Power Supply #2	12.50 ( $\lambda_{C2}$ )	Vendor Supplied
3.	Power Supply #3	71.43 ( $\lambda_{C3}$ )	Vendor Supplied
4.	Master Timing Unit (MTU)	64.72 ( $\lambda_{C4}$ )	MIL-HDBK-217B, Section 3
5.	CCU Central Processor Card	78.60 ( $\lambda_{C5}$ )	MIL-HDBK-217B, Section 3
6.	CCU I/O Card No. 1	14.01 ( $\lambda_{C6}$ )	MIL-HDBK-217B, Section 3
7.	CCU I/O Card No. 2	14.01 ( $\lambda_{C7}$ )	MIL-HDBK-217B, Section 3
8.	CCU I/O Card No. 3	35.50 ( $\lambda_{C8}$ )	MIL-HDBK-217B, Section 3

\*Assuming B-2 Quality Level



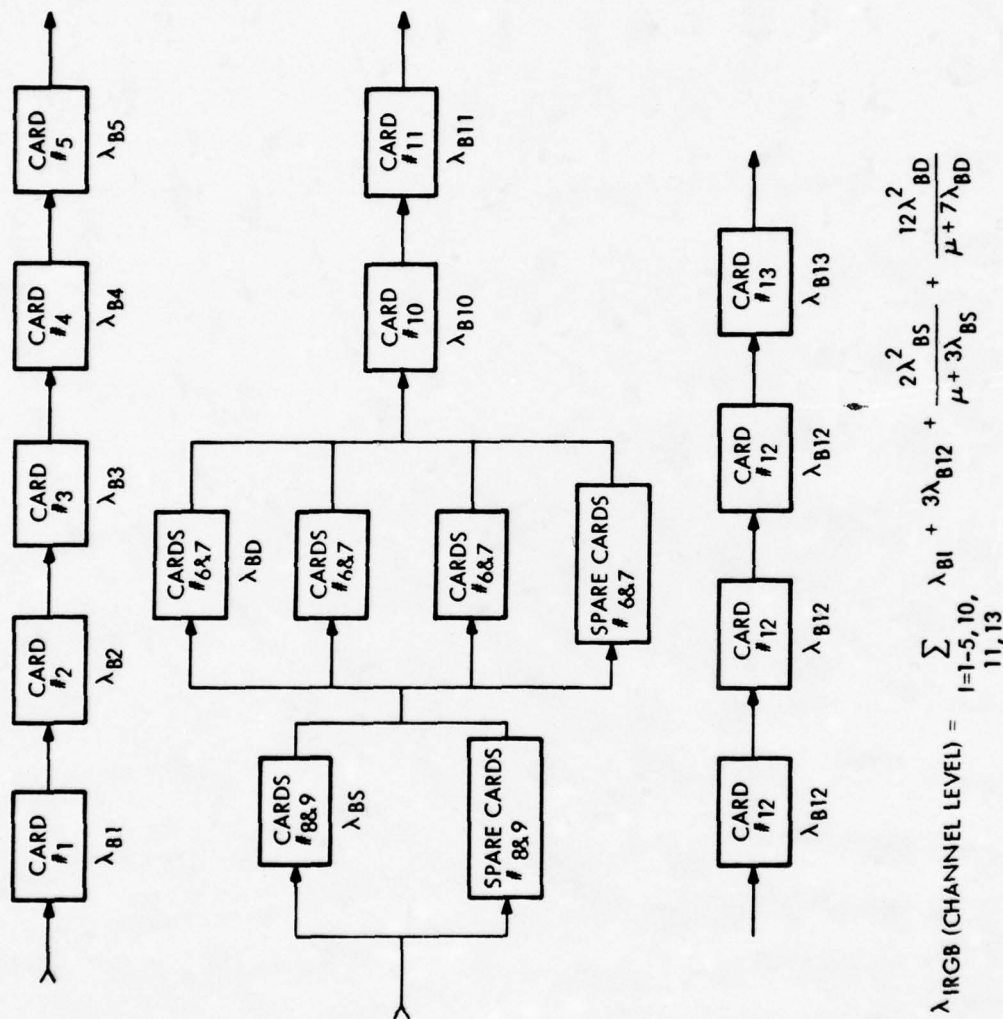


$$\lambda_{\text{IRGA (CHANNEL LEVEL)}} = \sum_{i=1,2,3,8,9,10} \lambda_{A_i} + \frac{2\lambda_{A4}^2}{\mu + 3\lambda_{A4}} + \frac{2\lambda_{AM}^2}{\mu + 3\lambda_{AM}}$$

## NOTES:

1.  $1/\mu$  EQUALS MEAN-TIME-TO-RESTORE SERVICE
2.  $\lambda_{AM} = \lambda_{A5} + \lambda_{A6} + \lambda_{A7}$
3. SEE TABLE 7-45 FOR CARD DESCRIPTIONS AND ASSOCIATED FAILURE RATES

Figure 7-54. Basic IRGA Reliability Block Diagram

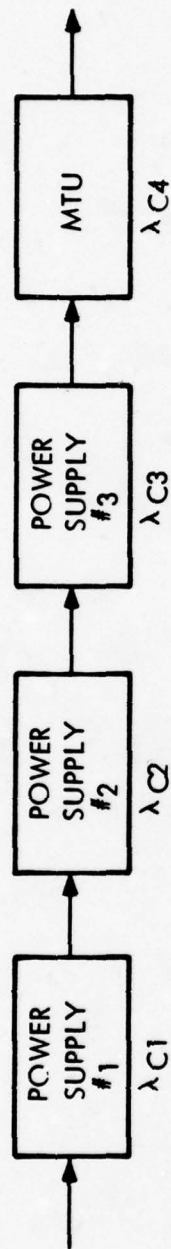


NOTES:

1.  $1/\mu$  EQUALS MEAN-TIME-TO-RESTORE SERVICE
2. SEE TABLE 7-46 FOR CARD DESCRIPTIONS AND ASSOCIATED FAILURE RATES

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Figure 7-55. Basic IRGB Reliability Block Diagram



$$\lambda_{CEG} = \sum_{i=1}^4 \lambda_{Ci}$$

NOTE: SEE TABLE 7-47 FOR COMPONENT FAILURE RATES

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Figure 7-56. Basic CEG Reliability Block Diagram

The reliability of each group in terms of the failure rates of its components is specified in each figure. The channel reliability of the DCE is given by the sum of the group reliabilities. Using the estimated failure rates in Tables 7-45 through 7-47, the group reliabilities are calculated to be as shown in Table 7-48.

TABLE 7-48. BASIC EQUIPMENT CHANNEL RELIABILITIES

EQUIPMENT GROUP	RELIABILITY (1/HR.)
IRGA	$1.179 \times 10^{-4}$ (IRGA)
IRGB	$2.133 \times 10^{-4}$ (IRGB)
CEG	$1.686 \times 10^{-4}$ (CEG)

Implicit in this calculation is the assumption that the mean-time-to-restore service,  $1/u$ , for failures within non-redundant elements and for double failures within redundant functions is 30 minutes. This includes a 5 minute mean-time-to-repair (card substitution) and a 25 minute mean-coordination-time for technical controllers and maintenance personnel. For the purposes of this section, it is further assumed that DCEs are placed at attended stations and that extensive travel time is not a consideration.

DCE availability is merely the product of the three equipment group availabilities, that is:

$$A_{DCE} = A_{IRGA} \cdot A_{IRGB} \cdot A_{CEG}$$

Each group availability is related to its reliability by the formula:

$$A = u/(u + \lambda)$$

where  $u$  is the reciprocal of mean-time-to-restore service, defined previously. Substituting the values for  $\lambda$  and  $u$  calculated above gives

$$\begin{aligned} A_{DCE} &= A_{IRGA} \cdot A_{IRGB} \cdot A_{CEG} \\ &= (0.999941) (0.999893) (0.999916) \\ &= 0.999750 \end{aligned}$$

This availability does not meet the DCE requirement of 0.99999167. In order to satisfy this requirement, it will be necessary to increase equipment redundancy over that specified in the basic design; the desired degree of redundancy is determined in the next section.



### 7.4.3 DCE Redundancy Requirements

In order to accurately specify redundancy requirements, it is necessary to refine the availability analysis of Section 4.6 so that individual DCE equipment group availability requirements can be specified. This will result in the DCE station availability being a function of the actual equipment groups deployed; however, the total DNC unavailability contribution to the DCS reference channel will not exceed 0.00005, as required.

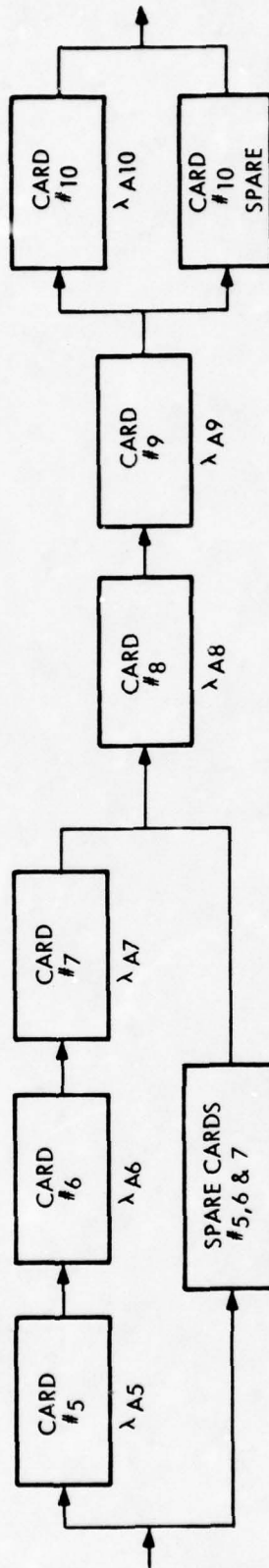
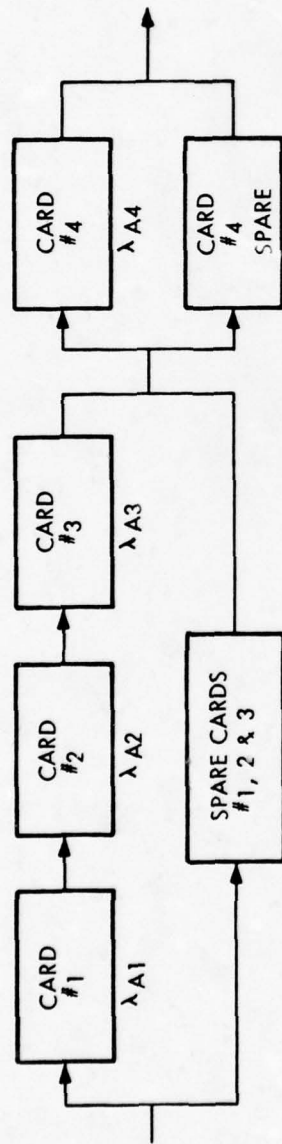
The analysis of Section 4.6 is based on the assumption that all three DCE equipment groups are deployed at each station receiving DNC hardware. In almost all DNC applications, through, no more than two IRGBs will be required, one at each terminal station of a channel. Referring to Section 4.6, the DCS reference channel includes six stations with DNC hardware. The assumed DCE equipment distribution in the reference channel is an IRGA and a CEG at each of four intermediate stations and an IRGA, an IRGB and a CEG at each of the two terminal stations. Assuming that the three DCE equipment groups have approximately the same basic reliability, which is consistent with the results of Section 7.4.2, the per group unavailability requirement is given by  $0.00005/14 = 3.57 \times 10^{-6}$ . The resulting DCE equipment group (IRGA, IRGB and CEG) channel availability requirement is given by  $(1 - 0.00005/14)$  or .9999964.

The equipment group availability requirement equates to a failure rate of no greater than  $7.14286 \times 10^{-6}$ , assuming as before that the mean-time-to-restore service is 30 minutes. By referring to Tables 7-45 through 7-47, it may be seen that most of the components of the three equipment groups individually exceed this failure rate requirement. Thus, it will be necessary to add redundancy to these components in order to bring the overall failure rates of the groups within specification. Figures 7-57 through 7-59 illustrate the additional redundancy required over the basic DCE design in order to satisfy requirements. The redundancy paths have been grouped over cards of similar function so as to simplify the complexity of standby element switching. The redundant elements are in a 1:N configuration, where N is the number of elements necessary to provide for the maximum size equipment group. Basic DCE modularity is unaffected by the redundancy.

The equipment group reliabilities and availabilities which result from the added redundancy are shown in Table 7-49.

TABLE 7-49. DCE CHANNEL RELIABILITY/AVAILABILITY WITH ADDITIONAL REDUNDANCY

EQUIPMENT GROUP	RELIABILITY	AVAILABILITY
IRGA	$5.471 \times 10^{-6}$	0.9999972
IRGB	$5.362 \times 10^{-6}$	0.9999973
CEG	$9.846 \times 10^{-9}$	> 0.9999999

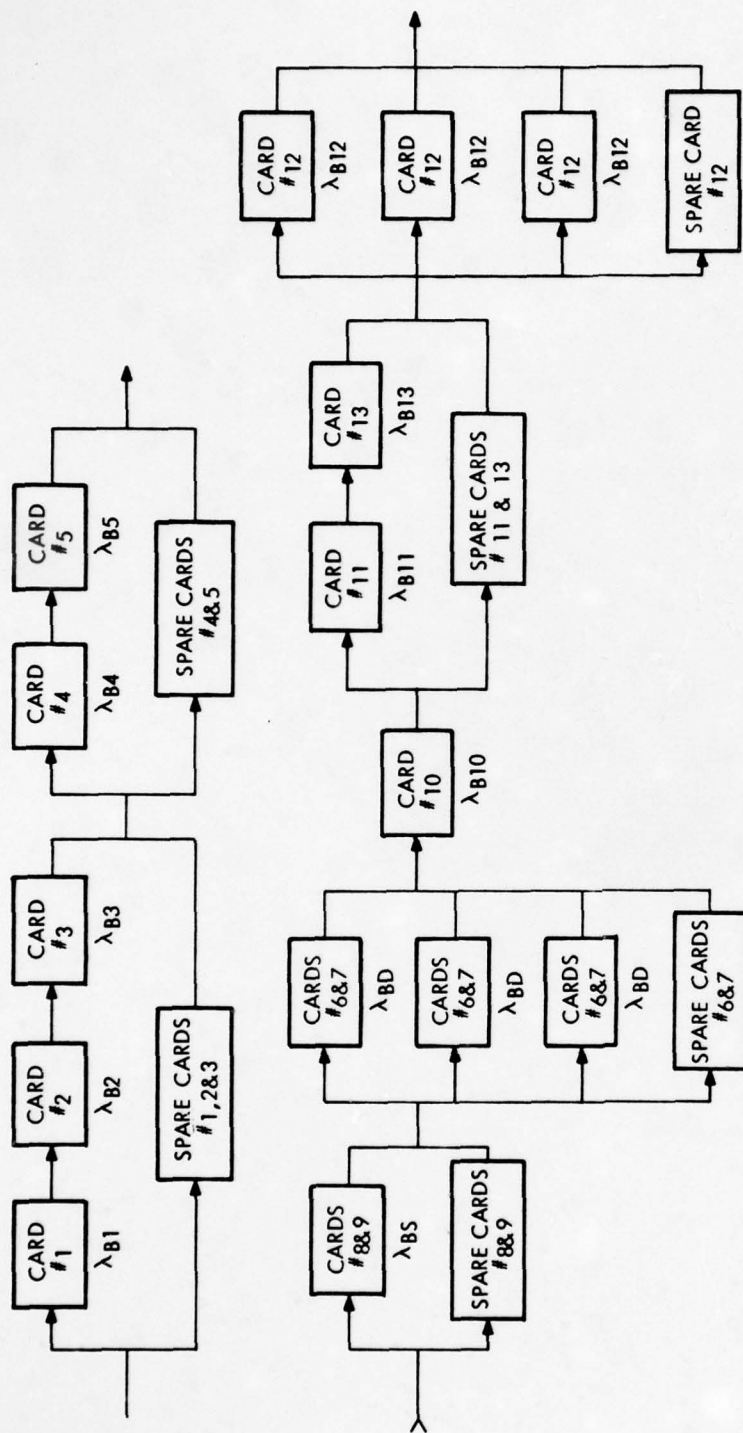


$$\lambda_{IRGA} \text{ (CHANNEL LEVEL)} = \frac{2 \lambda^2 A_F}{\mu + 3 \lambda A_F} + \frac{2 \lambda^2 A_4}{\mu + 3 \lambda A_4} + \frac{2 \lambda^2 A_M}{\mu + 3 \lambda A_M} + \frac{2 \lambda^2 A_{10}}{\mu + 3 \lambda A_{10}} + \sum_{i=8,9} \lambda A_i$$

## NOTES:

1.  $1/\mu$  EQUALS MEAN-TIME-TO-RESTORE SERVICE
2.  $\lambda_{AF} = \lambda A_1 + \lambda A_2 + \lambda A_3$
3.  $\lambda_{AM} = \lambda A_5 + \lambda A_6 + \lambda A_7$
4. SEE TABLE 7-45 FOR CARD DESCRIPTIONS AND ASSOCIATED FAILURE RATES

Figure 7-57. IRGA With Additional Redundancy - Reliability Block Diagram



$$\lambda_{\text{IRGB}} (\text{CHANNEL LEVEL}) = \frac{2\lambda_{\text{BF}}^2}{\mu + 3\lambda_{\text{BF}}} + \frac{2\lambda_{\text{BM}}^2}{\mu + 3\lambda_{\text{BM}}} + \frac{2\lambda_{\text{BS}}^2}{\mu + 3\lambda_{\text{BS}}} + \frac{12\lambda_{\text{BD}}^2}{\mu + 7\lambda_{\text{BD}}} + \frac{2\lambda_{\text{BO}}^2}{\mu + 3\lambda_{\text{BO}}} + \frac{12\lambda_{\text{B12}}^2}{\mu + 7\lambda_{\text{B12}}}$$

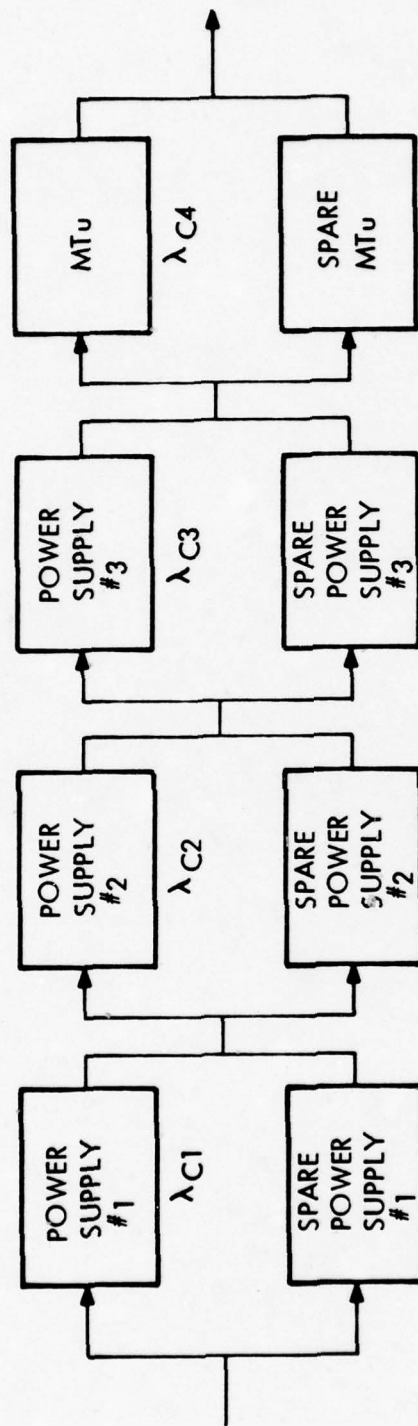
## NOTES:

1.  $1/\mu$  EQUAL MEAN-TIME-TO-RESTORE SERVICE2.  $\lambda_{\text{BF}} = \lambda_{\text{B1}} + \lambda_{\text{B2}} + \lambda_{\text{B3}}$ 3.  $\lambda_{\text{BM}} = \lambda_{\text{B4}} + \lambda_{\text{B5}}$ 4.  $\lambda_{\text{BO}} = \lambda_{\text{B11}} + \lambda_{\text{B13}}$ 

5. SEE TABLE 7-46 FOR CARD DESCRIPTIONS AND ASSOCIATED FAILURE RATES

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Figure 7-58. IRGB With Additional Redundancy - Reliability Block Diagram



$$\lambda_{CEG} = \frac{2\lambda^2_{C1}}{\mu + 3\lambda_{C1}} + \frac{2\lambda^2_{C2}}{\mu + 3\lambda_{C2}} + \frac{2\lambda^2_{C3}}{\mu + 3\lambda_{C3}} + \frac{2\lambda^2_{C4}}{\mu + 3\lambda_{C4}}$$

NOTES:

1.  $1/\mu$  EQUALS MEAN-TIME-TO-RESTORE SERVICE
2. SEE TABLE 7-47 FOR COMPONENT FAILURE RATES

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Figure 7-59. CEG with Redundancy - Reliability Block Diagram



These values are based on the reliability formulae in Figures 7-57 through 7-59 and the component failure rates tabularized in Section 7.4.1. As may be seen from Table 7-49, each DCE equipment group with the specified degree of redundancy satisfies the group availability requirement of 0.9999964.

Two other reliability factors have been estimated based on the additional DCE redundancy. They are mean-time-between-incidents (MTBI) and mean-time-between-catastrophic failures (MTBC). The former denotes the mean-time between any equipment failure, on-line or redundant, and is simply a function of the total quantity of components employed. The MTBI for each of the DCE equipment groups in its maximum configuration is given below in Table 7-50.

TABLE 7-50. DCE MEAN-TIME-BETWEEN-INCIDENTS

EQUIPMENT GROUP	MTBI (HR.)
IRGA (192 Digital Groups)	220
IRGB (50 Digital Groups)	424
CEG	2275

MTBC for the DCE has been defined as the mean-time between failures which affect more than one-third of the system (i.e., greater than 33 percent system degradation). MTBC has been estimated for the three equipment groups in their maximum configuration and the results are given below in Table 7-51.

TABLE 7-51. DCE MEAN-TIME-BETWEEN-CATASTROPHIC FAILURES

EQUIPMENT GROUPS	MTBC (HR.)
IRGA (192 Digital Groups)	$232.56 \times 10^3$
IRGB (50 Digital Groups)	$188.22 \times 10^3$
CEG	$101.56 \times 10^6$

It should be noted that the effectiveness of hardware redundancy is highly dependent on fault detection and isolation routines employed. The DCE uses both hardware and software fault control techniques to isolate failures to either the card or subassembly level. The basic techniques include: hardware and software parity checking of data and commands, on-line/off-line comparisons, hardware lockout, scanning of status indicators such as FIFO buffer overflow/underflow, and diagnostic software routines. A description of the implementation of these techniques is included in the hardware and software design sections.

#### 7.4.4 Preliminary Maintenance Concept

A preliminary maintenance concept for DNC is presented to establish guidelines that will be used at organizational, intermediate, and depot maintenance levels. A minimum system downtime at a reasonable support cost can be achieved using these maintenance levels as described below.

Organizational Level (OL) Maintenance is that maintenance performed by operating and maintenance (O&M) personnel who are part of the using organization. DNC equipment will be of modular design having self-test features and fault indicators to detect system failures. Fault isolation to the failed Line Replacement Units (LRU), will be accomplished via indicators either directly or in conjunction with diagnostic procedures. Repair will be accomplished by LRU replacement. A complement of ready spares will be provided with the DNC equipment.

Intermediate Level (IL) Maintenance is that maintenance performed by personnel responsible for direct support of the using organizations. The maintenance activity at this level will consist of replacement or panel mounted compartments. The repair of power modules will be by replacement of switches, connectors, wired-in PCBs, cables. Some PCBs will be repaired at this level. Intermediate maintenance personnel will also provide technical assistance to using organizations.

Depot Level (DL) Maintenance is that maintenance performed by personnel to support the two lower maintenance levels. The maintenance activity will consist of the testing and repair of plug-in PCBs and power supply modules. It will also cover the repair of internal wiring of the DNC equipment, which includes wirewrap and soldering. In addition, this activity will be concerned in the rebuilding of damaged DNC equipment, which includes front and rear panels, connector plates and case replacement. A DNC PCB tester will be used for the checkout of repaired cards. An automatic tester will be used for the test and fault isolation of components on the PCBs.

## SECTION 8

### ILLUSTRATIVE APPLICATION OF DIGITAL NETWORK CONTROL

In this section, an example of the application of DNC to a digital network is presented. The example considers a network model based on DCEC furnished information pertaining to DEB, AUTOSEVOCOM II and TRI-TAC. Five DNC application alternatives are defined based on the DNC application factors discussed in Section 4. The alternatives are evaluated with respect to equipment requirements, performance, and acquisition costs. The preferred alternative is determined and corresponding physical requirements presented.

#### 8.1 NETWORK MODEL DESCRIPTION

The network model to be analyzed consists of digital multiplexing, transmission, and switching equipment planned as part of the DEB and AUTOSEVOCOM II networks in southern Germany. Network connectivity is illustrated in Figure 8-1; station and link descriptions are provided in Tables 8-1 and 8-2, respectively.

The model includes two AUTOSEVOCOM II switches located at DON and LKF, and three DAXs located at BHR, SEH and RSN. The associated interswitch trunking is shown in Figure 8-2. The model also includes a TRI-TAC trunking requirement as shown in Figure 8-3. T1 digital group routing is shown in Tables 8-3 and 8-4. Table 8-3 lists those digital groups which are totally within the model. Table 8-4 lists those digital groups which have either one or both terminal stations outside the model; the routing outside the model is not shown and is not a consideration in the present analysis.

#### 8.2 DNC APPLICATION ALTERNATIVES

The illustrative application of DNC to the network model will consider five alternatives based on the modularity and performance factors discussed in Section 4. The five alternatives are

- a. Partial Interconnect
- b. Full Interconnect
- c. Partial Flexibility
- d. Full Flexibility
- e. Maximum Full Flexibility

and each is labeled according to the network deployment algorithm (see Section 4.3) employed to determine the placement of DNC hardware in the model.

Table 8-5 specifies the DCE equipment groups required at each station in the network model for each alternative.

All alternatives require an IRGB at each station which has AII or TRI-TAC requirements. As may be seen from Figures 8-2 and 8-3,



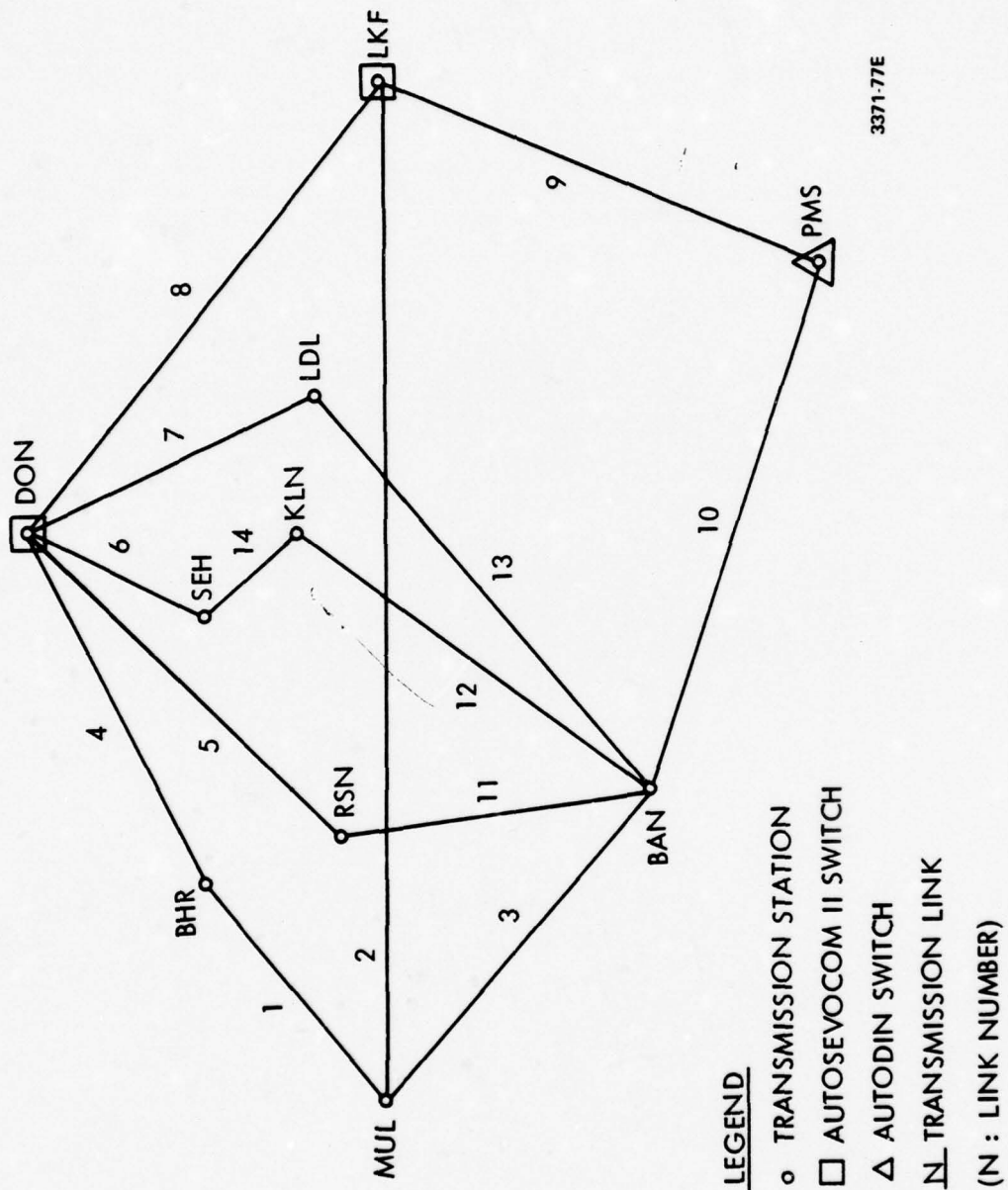


Figure 8-1. Network Model Connectivity

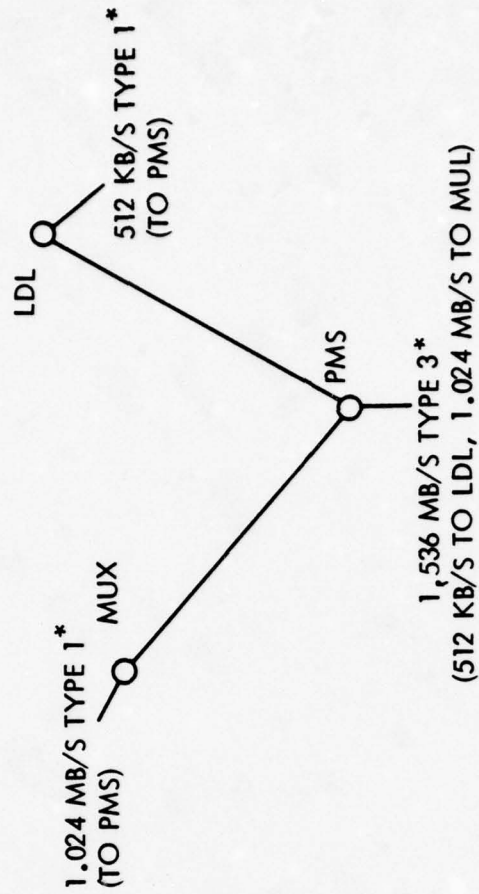
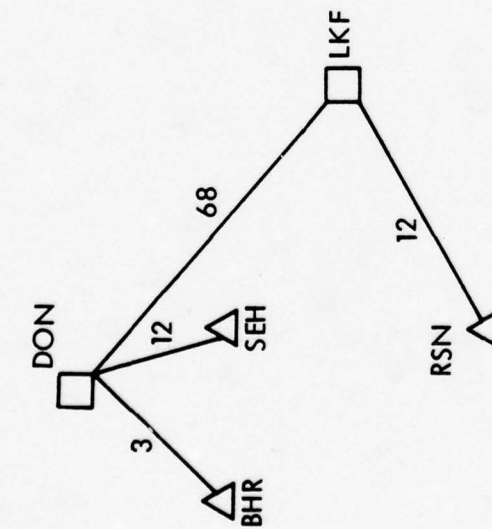


TABLE 8-1. STATION DESCRIPTIONS

STATION		ATEC ELEMENTS
1. Bann	(BAN)	MAS, NCS
2. Baum Holden	(BHR)	MAS
3. Donnersberg	(DON)	MAS, NCS
4. Kaiserslautern	(KLN)	MAS
5. Landstuhl	(LDL)	MAS
6. Langerkopf	(LKF)	MAS, NCS
7. Muhl	(MUL)	MAS
8. Pirmasens	(PMS)	MAS
9. Ramstein	(RMS)	MAS
10. Sembach	(SEH)	MAS

TABLE 8-2. LINK DESCRIPTIONS

TERMINATING STATIONS	LINK NUMBER	MILEAGE
MUL - BHR	1	13.4
MUL - LKF	2	45
MUL - BAN	3	37
BHR - DON	4	32
DON - RSN	5	21
DON - SEH	6	7
DON - LDL	7	23
DON - LKF	8	23
LKF - PMS	9	12
PMS - BAN	10	13
BAN - RSN	11	5
BAN - KLN	12	10.2
BAN - LDL	13	23
KLN - SEH	14	6.5



\* FORMATS DEFINED IN TRI-TAC INTERFACE CONTROL DRAWING ICD-003

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Figure 8-2. AUTOSEVOCOM II  
Trunking Requirements

Figure 8-3. TRI-TAC Digital Group  
Requirements

TABLE 8-3. INTRA-NETWORK MODEL T1 DIGITAL GROUP ROUTING

	TERMINATING STATIONS	DIGITAL GROUP ROUTING										NUMBER OF GROUPS
		B A N	B H R	D O N	K L N	L D L	L K F	M U L	P M S	R S N	S E H	
1	BAN - MUL	X						X				3
2	BAN - LKF	X					X	X				2
3	BAN - PMS	X							X			1
4	BAN - LKF	X					X		X			2
5	BAN - SEH	X			X						X	1
6	BAN - KLN	X			X							2
7	BAN - RSN	X								X		6
8	BAN - LDL	X				X						1
9	BHR - KLN	X	X		X			X				1
10	BHR - DON		X	X								1
11	BHR - KLN		X	X	X						X	1
12	DON - SEH			X							X	1
13	DON - KLN			X	X						X	1
14	DON - LKF			X			X					5
15	DON - PMS			X			X		X			4
16	DON - RSN			X						X		5
17	DON - PMS	X		X					X	X		1
18	KLN - RSN	X			X					X		2
19	LDL - RSN			X		X				X		1
20	LDL - LKF	X				X	X		X			1
21	LDL - PMS	X				X			X			1
22	LDL - MUL	X				X		X				1
23	LKF - MUL						X	X				3
24	LKF - PMS						X		X			3
25	LKF - RSN	X					X		X	X		1
26	LKF - SEH	X			X		X		X		X	1
27	MUL - SEH		X	X				X			X	1
28	MUL - RSN	X						X		X		1
29	RSN - SEH			X						X	X	1
30	RSN - SEH	X			X					X	X	1

TABLE 8-4. INTER-NETWORK MODEL T1 DIGITAL GROUP ROUTING

	TERMINATING STATIONS	DIGITAL GROUP ROUTING													NUMBER OF GROUPS
		B	B	D	K	L	L	M	P	R	S				
		A	H	O	L	D	K	U	M	S	E				
		N	R	N	N	L	F	L	S	N	H				
31	BAN - SCH	X							X						1
32	BAN - FEL	X		X						X					1
33	DON - FEL		X	X				X							2
34	DON - SCH		X	X				X							1
35	FEL - RSN			X						X					1
36	FEL - LDL			X		X									2
37	HAN - RSN		X	X				X		X					1
38	LKF - SCH							X	X						1
39	PMS - SCH	X						X	X						1
40	RSN - SCH	X						X		X					1
41	PMS - LFD	X		X		X				X					1
42	DON - HST			X				X							1
43	KLN - FKT	X			X			X							1
44	KLN - FKT			X	X						X				1
45	KLN - HDG			X	X						X				3
46	KLN - SGT			X	X						X				1
47	KLN - KSL			X	X						X				1
48	KLN - NBG			X	X						X				1
49	LDL - SGT			X		X	X								1
50	LKF - HIN							X	X						1
51	PMS - SGT							X		X					1
52	RSN - SGT	X						X		X	X				1
53	MAS - HIN	X							X	X					1
54	MAS - SGT							X		X					1

WHERE:

FEL - Feldberg

FKT - Frankfurt

HAN - Hann

HDG - Heidelberg

HIN - Hillingdon

HST - Hohenstadt

KSL - Koenigstuhl

LFD - Lohnsfeld

MAS - Mass Weiller

NBG - Nuerberg

SCH - Schoenfeld

SGT - Stuttgart

## NOTES:

1. Routes 31 through 52 have one terminating station within the network model.
2. Routes 52 and 53 have neither terminating station within the network model.



TABLE 8-5. DCE DEPLOYMENT FOR DNC ALTERNATIVES

STATION	DNC ALTERNATIVE			
	PARTIAL INTERCONNECT	FULL INTERCONNECT	PARTIAL FLEXIBILITY	FULL FLEXIBILITY
BAN	NE	A, C	A, C	A, C
BHR	B, C	B, C	B, C	A, B, C
DON	A, B, C	A, B, C	A, B, C	A, B, C
KLN	NE	NE	NE	A, C
LDL	B, C	B, C	B, C	A, B, C
LKF	B, C	A, B, C	A, B, C	A, B, C
MUL	B, C	B, C	A, B, C	A, B, C
PMS	B, C	B, C	B, C	A, B, C
RSN	B, C	B, C	B, C	A, B, C
SEH	B, C	B, C	A, B, C	A, B, C

A: INTERFACE AND REASSIGNMENT GROUP A  
 B: INTERFACE AND REASSIGNMENT GROUP B  
 C: COMMON EQUIPMENT GROUP  
 NE: NO EQUIPMENT REQUIRED

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this includes all stations except BAN and KLN. The placement of IRGAs varies between the alternatives and this variation reflects the degree of network flexibility achieved with respect to restoration, reconfiguration and performance assessment. A CEG is required at any station with an IRGA or an IRGB.

With respect to IRGA usage, it is assumed that each IRGA provides up to 1.544 Mb/s of capacity for use by ATEC in the performance assessment functions (drop and insert of any test signal which is TD-1192 compatible) and up to 3.088 Mb/s of capacity for the drop and insert of message channels. Similarly, IRGB sizing includes 3.088 Mb/s of capacity for both ATEC performance assessment and drop and insert of message channels. Although this capacity has been allocated for specific purposes, the flexibility of the DCE design permits it to be used for any purpose such as rechannelization, testing, etc. Based on AII and TRI-TAC requirements, a single 1.544 Mb/s bit stream will be used to interconnect an IRGA and IRGB at stations where they are jointly deployed. From these operational considerations and the deployment algorithm definitions in Section 4.3, the required per station DCE size requirements in units of Tls are shown in Table 8-6 for each deployment option. Associated IRGA and IRGB card requirements are given in Tables 8-7 through 8-12.

As shown by Tables 8-6 and 8-12, the locations and sizes of the IRGBs required in the network model are independent of the DNC alternative selected. All alternatives require eight IRGBs, BAN and KLN being the two sites which do not receive one. This is due to the fact that IRGB deployment, in order to be cost-effective as discussed in Section 4.2, is primarily limited to AII and TRI-TAC interfacing. Implementation issues associated with the IRGA are discussed in the following sections.

#### 8.2.1 Partial Interconnect Alternative

The partial interconnect alternative provides the fewest capabilities of the five alternatives. It permits at least 24 channels to be automatically established between any two stations over a preestablished route. However, manual patching may be required at the two terminal stations to complete the connection. As shown in Table 8-5, this approach requires a single IRGA at DON and an IRGB at each location except BAN and KLN. Based on the partial interconnect algorithm, for each station in the network model, one digroup which terminates at that station must pass through an IRGA and all IRGAs must be connected. Although other configurations are possible, placement of the IRGA at DON meets this requirement with the minimum DNC hardware. The IRGA at DON interfaces with six network digital groups, Tls 11, 14, 15, 19, 27, and 32 where the numbers are referenced to Tables 8-3 and 8-4. This set of Tls ensures that each station has at least one Tl which passes through the DCE at DON.

TABLE 8-6. DCE STATION SIZES IN T1 DIGITAL GROUPS

STATION	DNC ALTERNATIVE									
	PARTIAL INTERCONNECT		FULL INTERCONNECT		PARTIAL FLEXIBILITY		FULL FLEXIBILITY		MAXIMUM FULL FLEXIBILITY	
	IRGA	IRGB	IRGA	IRGB	IRGA	IRGB	IRGA	IRGB	IRGA	IRGB
BAN	0	0	60	0	13	0	51	0	94	0
BHR	0	4	0	4	0	4	10	3	42	3
DON	16	3	60	3	14	3	56	3	154	3
KLN	0	0	0	0	0	0	28	0	54	0
LDL	0	4	0	4	0	4	20	3	28	3
LKF	0	6	62	3	10	3	48	3	84	3
MUL	0	4	0	4	8	3	24	3	86	3
PMS	0	6	0	6	0	6	30	3	50	3
RSN	0	4	0	4	0	4	48	3	60	3
SEH	0	4	0	4	8	3	20	3	40	3

IRGA: INTERFACE AND REASSIGNMENT GROUP A

IRGB: INTERFACE AND REASSIGNMENT GROUP B

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TABLE 8-7. IRGA CARD REQUIREMENTS FOR PARTIAL INTERCONNECT ALTERNATIVE

STATION	FRAMING UNIT CARD	DIGROUP BUFFER CARD	FRAME ALIGN. CARD	CHANNEL SELECTOR CARD	DMU CARD	OCU ADDRESS MEMORY CARD	OCU CONTROL CARD	OFU CARD NO. 1	OFU CARD NO. 2	OFU CARD NO. 3
BAN	0	0	0	0	0	0	0	0	0	0
BHR	1	1	1	0	0	0	0	0	0	0
DON	4	4	4	2	2	2	2	1	1	2
KLN	0	0	0	0	0	0	0	0	0	0
LDL	1	1	1	0	0	0	0	0	0	0
LKF	1	1	1	0	0	0	0	0	0	0
MUL	1	1	1	0	0	0	0	0	0	0
PMS	1	1	1	0	0	0	0	0	0	0
RSN	1	1	1	0	0	0	0	0	0	0
SEH	1	1	1	0	0	0	0	0	0	0

NOTE: Card counts shown for basic DCE design. For additional redundancy design increment Framing Unit, Digroup Buffer, Frame Align and OFU Card No. 3 card counts by one.



TABLE 8-8. IRGA CARD REQUIREMENTS FOR FULL INTERCONNECT ALTERNATIVE

STATION	FRAMING UNIT CARD	DIGROUP BUFFER CARD	FRAME ALIGN. CARD	CHANNEL SELECTOR CARD	DMU CARD	OCU ADDRESS MEMORY CARD	OCU CONTROL CARD	OFU CARD NO. 1	OFU CARD NO. 2	OFU CARD NO. 3
BAN	12	12	12	2	6	3	3	1	1	8
BHR	1	1	1	0	0	0	0	0	0	0
DON	12	12	12	2	6	3	3	1	1	8
KLN	0	0	0	0	0	0	0	0	0	0
LDL	1	1	1	0	0	0	0	0	0	0
LKF	13	13	13	2	6	3	3	1	1	8
MUL	1	1	1	0	0	0	0	0	0	0
PMS	1	1	1	0	0	0	0	0	0	0
RSN	1	1	1	0	0	0	0	0	0	0
SEH	1	1	1	0	0	0	0	0	0	0

NOTE: Card counts shown for basic DCE design. For additional redundancy design increment Framing Unit, Digroup Buffer, Frame Align and OFU Card No. 3 card counts by one.

TABLE 8-9. IRGA CARD REQUIREMENTS FOR PARTIAL FLEXIBILITY

STATION	FRAMING UNIT CARD	DIGROUP BUFFER CARD	FRAME ALIGN. CARD	CHANNEL SELECTOR CARD	DMU CARD	OCU ADDRESS MEMORY CARD	OCU CONTROL CARD	OFU CARD NO. 1	OFU CARD NO. 2	OFU CARD NO. 3
BAN	3	3	3	2	2	2	2	1	1	2
BHR	1	1	1	0	0	0	0	0	0	0
DON	3	3	3	2	2	2	2	1	1	2
KLN	0	0	0	0	0	0	0	0	0	0
LDL	1	1	1	0	0	0	0	0	0	0
LKF	2	2	2	2	2	2	2	1	1	2
MUL	2	2	2	2	2	2	2	1	1	2
PMS	1	1	1	0	0	0	0	0	0	0
RSN	1	1	1	0	0	0	0	0	0	0
SEH	2	2	2	2	2	2	2	1	1	1

NOTE: Card counts shown for basic DCE design. For additional redundancy design increment Framing Unit, Digroup Buffer, Frame Align and OFU Card No. 3 card counts by one.

TABLE 8-10. IRGA CARD REQUIREMENTS FOR FULL FLEXIBILITY

STATION	FRAMING UNIT CARD	DIGROUP BUFFER CARD	FRAME ALIGN. CARD	CHANNEL SELECTOR CARD	DMU CARD	OCU ADDRESS MEMORY CARD	OCU CONTROL CARD	OFU CARD NO. 1	OFU CARD NO. 2	OFU CARD NO. 3
BAN	10	10	10	2	6	3	3	1	1	7
BHR	2	2	2	2	2	2	2	1	1	2
DON	12	12	12	2	6	3	3	1	1	7
KLN	6	6	6	2	2	2	2	1	1	4
LDL	4	4	4	2	2	2	2	1	1	3
LKF	10	10	10	2	6	3	3	1	1	6
MUL	5	5	5	2	2	2	2	1	1	3
PMS	6	6	6	2	2	2	2	1	1	4
RSN	10	10	10	2	6	3	3	1	1	6
SEH	4	4	4	2	2	2	2	1	1	3

NOTE: Card counts shown for basic DCE design. For additional redundancy design increment Framing Unit, Digroup Buffer, Frame Align and OFU Card No. 3 card counts by one.

TABLE 8-11. IRGA CARD REQUIREMENTS FOR MAXIMUM FULL FLEXIBILITY

STATION	FRAMING UNIT CARD	DIGROUP BUFFER CARD	FRAME ALIGN. CARD	CHANNEL SELECTOR CARD	DMU CARD	OCU ADDRESS MEMORY CARD	OCU CONTROL CARD	OFU CARD NO. 1	OFU CARD NO. 2	OFU CARD NO. 3
BAN	19	19	19	2	12	4	4	1	2	12
BHR	9	9	9	2	6	3	3	1	1	6
DON	31	31	31	2	30	6	6	1	3	20
KLN	11	11	11	2	6	3	3	1	1	7
LDL	6	6	6	2	2	2	2	1	1	4
LKF	10	10	10	2	12	4	4	1	2	11
MUL	5	5	5	2	12	4	4	1	2	11
PMS	6	6	6	2	6	3	3	1	1	7
RSN	10	10	10	2	6	3	3	1	1	8
SEH	4	4	4	2	6	3	3	1	1	5

NOTE: Card counts shown for basic DCE design. For additional redundancy design increment Framing Unit, Digroup Buffer, Frame Align and OFU Card No. 3 card counts by one.



TABLE 8-12. IRGB CARD REQUIREMENTS FOR ALL ALTERNATIVES

STATION	FRAMING UNIT CARD	DIGROUP BUFFER CARD	FRAME ALIGN. CARD	MUX & CONV. CARD	MUX. CONTROL CARD	BDMU CARD	BOCU CARD	OFCU CARD NO. 1	OFCU CARD NO. 2	OFCU CARD NO. 3	OFCU CARD NO. 4	SDMU CARD	SOCU CARD
BAN	0	0	0	0	0	0	0	0	0	0	0	0	0
BHR	1	1	1	1	1	4	4	1	1	1	1	2	2
DON	1	1	1	1	1	4	4	1	1	1	1	2	2
KLN	0	0	0	0	0	0	0	1	1	1	1	0	0
LDL	1	1	1	1	1	4	4	1	1	1	1	2	2
LKF	1	1	1	1	1	4	4	1	1	1	1	2	2
MUL	1	1	1	1	1	4	4	1	1	1	1	2	2
PMS	1	1	1	1	1	4	4	1	1	1	1	2	2
RSN	1	1	1	1	1	4	4	1	1	1	1	2	2
SEH	1	1	1	1	1	4	4	1	1	1	1	2	2

NOTE: Card counts shown for basic DCE design. For additional redundancy design, increment Framing Unit, Digroup Buffer, Frame Align, MUX & Conv., Mux Control, and OFU Card No. 2, 3 and 4 card counts by one.

### 8.2.2 Full Interconnect Alternative

This alternative permits a channel to be automatically established between any two first-level multiplex ports without the need for manual patching at the terminal stations; however, as with partial interconnect, the routing is predetermined and not all routes through the network are selectable. Full interconnect requires a minimum of three IRGAs, one at each DON, BAN and KLN. Eight IRGBs are required for interfacing AII and TRI-TAC. In this approach, all Tls must interface an IRGA. To minimize the number of IRGA inputs, only Tls which are used to interconnect the IRGAs will interface more than one IRGA. The interconnecting network model Tls are 20, 32, and 42.

### 8.2.3 Partial Flexibility Alternative

In general, this alternative requires that IRGAs be placed in the network such that any route can be selected for establishing a channel. As with partial interconnect, manual patching may be required at the terminal stations. Five IRGAs are required to realize partial flexibility. The placement of this equipment is DON, BAN, KLN, MUH and SEH. Eight IRGBs are required for interfacing AII and TRI-TAC.

As required by the partial flexibility algorithm, the IRGAs must be interconnected such that any route can be selected. The network model Tls which are used to satisfy this requirement are 2, 10, 17, 26, 27, 32, 41 and 48.

### 8.2.4 Full Flexibility Alternative

This is the most flexible of the four deployment algorithms in that it provides for total route selection and does not require manual patching. The implementation requires that at each site, all terminating digital groups pass through the IRGA at that site. In addition, certain thru-groups must pass through an IRGA in order to satisfy the partial flexibility requirements. The network model Tls used to realize the latter requirement are as follows: 18 (BAN), 26 (BAN), 27 (DON), 32 (DON), 42 (DON), and 49 (LDL). The station in parenthesis indicates the intermediate location at which the group passes through an IRGA.

### 8.2.5 Maximum Full Flexibility Alternative

This approach is a variation of the previous alternative in which all digital groups at a station, whether thru or terminating groups, pass through the IRGA at that station. Maximum full flexibility requires no manual patching and provides complete route selectivity down to the channel level.

## 8.3 NETWORK MODEL ACQUISITION COSTS

The acquisition cost of each DNC alternative is shown in Table 8-13 for the basic DCE design and in Table 8-14 for the additional

TABLE 8-13. ACQUISITION COSTS FOR DNC ALTERNATIVES  
BASED ON BASIC DCE DESIGN

Station	DNC ALTERNATIVE				
	Partial Interconnect	Full Interconnect	Partial Flexibility	Full Flexibility	Maximum Full Flexibility
BAN	0	99951	67253	99951	140010
BHR	63386	63386	63386	122139	154837
DON	122139	154837	122139	154837	274368
KLN	0	0	0	67253	99951
LDL	63386	63386	63386	122139	122139
LKF	63386	154837	122139	154837	194896
MUL	63386	63386	122139	122139	194896
PMS	63386	63386	63386	122139	154837
RSN	63386	63386	63386	154837	154837
SEH	63386	63386	122139	122139	154837
TOTAL	565841	789941	809353	1242410	1645608

TABLE 8-14. ACQUISITION COSTS FOR DNC BASED ON  
ADDITIONAL REDUNDANCY DESIGN

Station	DNC ALTERNATIVE				
	Partial Interconnect	Full Interconnect	Partial Flexibility	Full Flexibility	Maximum Full Flexibility
BAN	0	110084	77438	110084	151197
BHR	77815	77815	77815	142673	175319
DON	142673	175319	142673	175319	297087
KLN	0	0	0	77438	110084
LDL	77815	77815	77815	142673	142673
LKF	77815	175319	142673	175319	216432
MUL	77815	77815	142673	142673	216432
PMS	77815	77815	77815	142673	175319
RSN	77815	77815	77815	175319	175319
SEH	77815	77815	142673	142673	175319
TOTAL	687378	927390	959390	1426844	1835181



redundancy design. The costs are based on Figures 9-1 and 9-2 and the DCE sizes specified in Table 8-6. Costs for IRGAs and IRGBs in Table 8-6 which are not one of the costed configurations (32, 64, 96, 128, 160 and 192 for the IRGA, and 6, 12, 18 and 24 for the IRGB) are given by the next largest costed configuration. For example, the cost of a IRGA with 48 T1 digital group inputs is the same as the cost of a 64 input IRGA and may be obtained from Figure 9-1.

The ranking of the alternatives in decreasing order of acquisition cost is given by:

1. Maximum Full Flexibility
2. Full Flexibility
3. Full Interconnect
4. Partial Flexibility
5. Partial Interconnect.

#### 8.4 DNC ALTERNATIVE SELECTION

In this section the capabilities of the DNC alternatives are examined and an alternative recommended for network model application.

The advantages gained by the deployment of DNC in a network derive from both the added route selection (partial flexibility) and the automated patching (full interconnect) capabilities it provides. Partial interconnect as discussed in Section 4.3 offers very limited benefits and is therefore not recommended.

With respect to overall network routing flexibility, being able to automatically reroute around failures and stress conditions and to dynamically reconfigure the network in response to changing demands, results in increased channel availability and survivability. To achieve this increase in flexibility requires that DCEs be deployed to provide at least a partial flexibility capability. Other network benefits such as increased performance assessment capabilities, automating technical control functions, and minimizing backhauling require that DEC's be deployed to provide a full interconnect capability. It is apparent that in order to achieve the general benefits of DNC with respect to:

- a. Hardware Savings
- b. Manpower Savings
- c. Circuit Mileage Savings
- d. Increased Availability and Survivability,

both capabilities are required. It is therefore recommended that a full flexibility deployment be applied to the network model so that the maximum performance and operational benefits can be obtained. As may be seen in Tables 8-13 and 8-14, full flexibility can be achieved with an approximate 50 percent increase in acquisition cost over partial flexibility and is clearly the most desirable approach. It is not recommended that maximum full flexibility be considered because it offers no substantial operational cost benefits over full flexibility

(although it does provide increased routing flexibility) but requires a considerable increase in acquisition costs.

## 8.5 DNC APPLICATION SUMMARY

The previous section recommended that DEC's be deployed in the network model so as to realize a full flexibility capability. This deployment permits a channel to be established and dynamically routed between any two first-level multiplexer ports without manual patching. The placement of the DCE equipments in the network model for full flexibility is specified in Table 8-5; the IRGA and IRGB T1 size requirements are shown in Table 8-6; the card complement of the DCE is specified in Tables 8-7 through 8-12; and the associated DCE acquisition costs are given Tables 8-13 and 8-14. A physical description of the DCEs along with power requirements are given in Table 8-15. The power requirements are specified twenty percent above typical, and the DCE sizes are based on the rack and nest descriptions provided in Sections 7.2.3.2 and 7.2.3.3.

TABLE 8-15. DCE DESCRIPTIONS FOR FULL FLEXIBILITY

STATION	SIZE (Nests)	POWER REQUIREMENTS (Watts)
BAN	3	816
BHR	3	921
DON	4	1229
KLN	2	509
LDL	3	921
LKF	4	1229
MUL	3	921
PMS	3	921
RSN	4	1229
SEH	3	921

Control of the DCEs would be as specified in Section 6.2.2. During normal operation, commands would be received from the nodal control system levels at either BAN, DON or LKF; acknowledgment messages would be returned to the nodal control which originated the command as well as to any colocated station controllers. Local control would be through the station controller's TTY or VDU/KY. Should a local I/O terminal not be available through the station control interface, one would be required for back-up in the event of a loss of the telemetry channel to nodal control.

## 8.6 LIFE CYCLE COST CONSIDERATIONS

Life Cycle Cost (LCC) is a procurement technique which considers operating, maintenance and other costs of ownership as well as acquisition price. Within this section, the results of a limited LCC analysis are presented for the selected DNC alternative (full flexibility) and, for comparison purposes, the four other DNC alternatives.

LCC can be broken down into the following three cost categories:

- a. Research and Development
- b. Acquisition
- c. Operating and Support.

The research and development category covers all costs incurred during the concept initiation, validation and full-scale development phases of the program. These include costs of feasibility studies, engineering design, development fabrication, assembly and test of engineering prototype models, initial system evaluation, and associated documentation. The costs in this category terminate with the satisfactory completion of testing. Per the SOW, research and development costs were not included in the analysis. Acquisition costs refer to those program costs required beyond the development phase to introduce into operational use a new capability, to procure initial, additional or replacement equipment for operational forces, or to provide for major modifications at an existing capability. Operating and support costs include the costs of personnel, material, facilities, and other direct and indirect costs required to operate, maintain, and support the equipment/system during the operational phase. It includes the cost of all parts consumed in maintenance of the equipment as well as the costs of maintaining the necessary supply systems for parts, components, equipment and information.

The two cost categories being considered can be further broken down into subcategories, as follows:

- a. Acquisition Costs
  - 1. Uninstalled Equipment
  - 2. Initial Support
    - Program Management
    - Technical Data
    - Integration and Assembly
    - System Test and Coordination
    - Test Peculiar and Common Support Equipment
    - Initial Spare
    - Initial Training
    - Transportation
    - Installation on Site
  - 3. Facilities (not required as specified in SOW)
- b. Operating and Support Costs
  - 1. Organization Level (OL) Maintenance
  - 2. Intermediate Level (IL) and Depot Level (DL) Maintenance



3. Inventory Management

4. Replaceable Spares

The results of LCC analysis are shown in Tables 8-16 and 8-17. The costs are broken out for each of the subcategories described above.



TABLE 8-16. TEN YEAR LIFE CYCLE COSTS (LCC) FOR DNC ALTERNATIVES  
BASED ON BASIC DCE DESIGN

LCC SUBCATEGORY	DNC ALTERNATIVE				
	PARTIAL INTERCONNECT	FULL INTERCONNECT	PARTIAL FLEXIBILITY	FULL FLEXIBILITY	MAX. FULL FLEXIBILITY
UNINSTALLED EQUIPMENT	565841	789941	809353	1242410	1645608
INITIAL SUPPORT	877054	1224409	1254497	1925736	2550692
OL MAINTENANCE	5658	7899	8094	12424	16456
IL & DL MAINTENANCE	198044	276479	283274	434844	575963
INVENTORY MANAGEMENT	84876	118491	121403	186362	246841
REPLACEABLE SPARES	537549	750444	768885	1180290	1563328
TOTAL	2269022	3167663	3245506	4982066	6598888

TABLE 8-17. TEN YEAR LIFE CYCLE COSTS (LCC) FOR DNC ALTERNATIVES  
BASED ON ADDITIONAL REDUNDANCY DESIGN

LCC SUBCATEGORY	DNC ALTERNATIVE				
	PARTIAL INTERCONNECT	FULL INTERCONNECT	PARTIAL FLEXIBILITY	FULL FLEXIBILITY	MAX. FULL FLEXIBILITY
UNINSTALLED EQUIPMENT	687378	927390	959390	1426844	1835181
INITIAL SUPPORT	1065436	1437455	1487055	2211608	2844531
OL MAINTENANCE	6874	9274	9594	14268	18352
IL & DL MAINTENANCE	240582	324587	335787	499395	642313
INVENTORY MANAGEMENT	103107	139109	143909	214027	275277
REPLACEABLE SPARES	721747	973760	1007360	1498186	1926940
TOTALS	2825124	3811575	3943095	5864328	7542594

## SECTION 9

### PRODUCTION COSTS

Cost data for the modular building blocks of the DCE is presented in this section. The data was derived from estimates of materials and recurring fabrication costs. The information is presented such that it can be utilized directly to define the cost of a DCE configuration for any application to the European DCS.

DCE unit production costs are based on a total production quantity of 25 DCE systems. The production costs were divided into three major cost elements during the estimation process:

- a. DCE Power Supply - Cost Element No. 1
- b. DCE Printed Circuit Cards - Cost Element No. 2
- c. DCE Mechanical Hardware, Assembly and System Checkout - Cost Element No. 3.

The major cost aspects involved in each cost element are discussed in subsequent subsections.

Table 9-1 summarizes the DCE configurations for which unit production costs have been estimated.

#### 9.1 DCE POWER SUPPLY - COST ELEMENT NO. 1

The following process was used to estimate the DCE Power Supply cost for each of the ten DCE configurations in Table 9-1:

- a. The DCE Power Supply requirements were established by using the following tables:
  1. Table 7-33 - Summary of DCE CEG Power Requirements.
  2. Table 7-34 - DCE IRGA Power Requirements Versus Number of 1.544 Mb/s Digroup Inputs.
  3. Table 7-35 - DCE IRGB Power Requirements Versus Number of IFCU Output Digroups.
- b. Commercial power supplies were selected according to the derived power requirements and costs for these units were obtained from the power supply vendor.

TABLE 9-1. DCE CONFIGURATION

CONFIGURATION NUMBER	DESCRIPTION OF DCE CONFIGURATION
1	(IRGA: 32 Tl Digital Groups) Plus CEG
2	(IRGA: 64 Tl Digital Groups) Plus CEG
3	(IRGA: 96 Tl Digital Groups) Plus CEG
4	(IRGA: 128 Tl Digital Groups) Plus CEG
5	(IRGA: 160 Tl Digital Groups) Plus CEG
6	(IRGA: 192 Tl Digital Groups) Plus CEG
7	(IRGB: <sup>①</sup> 15 TRI-TAC Format Digital Groups) Plus CEG
8	(IRGB: <sup>②</sup> 25 TRI-TAC Format Digital Groups) Plus CEG
9	(IRGB: <sup>③</sup> 40 TRI-TAC Format Digital Groups) Plus CEG
10	(IRGB: <sup>④</sup> 50 TRI-TAC Format Digital Groups) Plus CEG

① Maximum of three 1.536 Mb/s TRI-TAC format digital groups (no other input digital groups)

② Maximum of six 1.536 Mb/s TRI-TAC format digital groups (no other input digital groups)

③ Maximum of nine 1.536 Mb/s TRI-TAC format digital groups (no other input digital groups)

④ Maximum of twelve 1.536 Mb/s TRI-TAC format digital groups (no other input digital groups)



## 9.2 DCE PRINTED CIRCUIT CARDS - COST ELEMENT NO. 2

For each of the 10 DCE configurations listed in Table 9-1, the cost of the DCE Printed Circuit Cards was estimated.

The following factors determine the unit production cost of a DCE Printed Circuit Card.

- a. Cost of the basic 6" by 10" printed wiring board (4 layer: power, ground, 2 signal layers).
- b. Cost of 112-pin card connector plus miscellaneous hardware such as nuts, bolts, washers, etc.
- c. Cost of labor for assembly and test of the card.
- d. Cost of the integrated circuits to populate the printed wiring board.

The number of DCE Printed Circuit Cards required for each DCE configuration was determined from the following tables:

- a. Table 7-9 - IFU Card Requirements Versus IRGA Size
- b. Table 7-13 - ADMU Card Requirements Versus IRGA Size
- c. Table 7-14 - AOCU Card Requirements Versus IRGA Size
- d. Table 7-15 - OFU Card Requirements Versus IRGA Size
- e. Table 7-23 - IFCU Card Requirements Versus IFCU Size
- f. Table 7-24 - BDMU Card Requirements Versus IFCU Size
- g. Table 7-25 - BOCU Card Requirements Versus IFCU Size
- h. Table 7-28 - OFCU Card Requirements Versus IFCU Size
- i. Table 7-29 - SDMU/SOCU Card Requirements Versus IFCU Size
- j. Table 7-30 - CCU Card Requirements
- k. Figure 7-39 - DCE Common Equipment Group (CEG)

## 9.3 DCE MECHANICAL HARDWARE, ASSEMBLY AND SYSTEM CHECKOUT - COST ELEMENT NO. 3

For each of the 10 DCE configurations listed in Table 9-1, Cost Element No. 3 was estimated as described below.

### 9.3.1 DCE Mechanical Hardware

The DCE Mechanical Hardware includes all DCE materials other than the DCE Printed Circuit Cards. The following listing provides the major categories of DCE Mechanical Hardware.

- a. DCE Cabinet
- b. Blower
- c. Cooling Air Plenum
- d. DCE I/O Connectors
- e. DCE Printed Circuit Card Nest Assemblies

- f. DCE Control Panel Assembly
- g. Miscellaneous Mounting Assemblies, Cable Supports, etc.
- h. DCE I/O Cable Fabrication and Material.

Cost factors within each of these categories depends on the DCE configuration.

#### 9.3.2 DCE Mechanical Assembly

An estimate was made for the unit production cost to completely assemble a DCE. This includes mounting all the mechanical assemblies in the DCE Cabinet and mounting all Printed Circuit Cards in the nests.

#### 9.3.3 System Checkout

An estimate was made for the unit production cost to checkout the fully assembled DCE System.

#### 9.3.4 Final Quality Assurance (FQA)

An estimate was made for the unit production cost to have the DCE System checked by the GTE Sylvania FQA department prior to delivery.

#### 9.3.5 Contractor Overheads

The contractor overheads were applied to the estimated direct production cost of the DCE. The contractor overheads consist of an industry average for the manufacturing and engineering overhead, general administration (G&A) and fee.

### 9.4 CONDITIONS AND ASSUMPTIONS

The estimate of DCE Printed Circuit Card costs assumes that a special circuit card test set will be used by GTE Sylvania to automatically check out each completed card. This test set and the programming of it (preparation of test tapes, etc.) is considered as a non-recurring cost and is not included in the unit production cost estimate.

The estimate of DCE System Checkout assumes that a special DCE test set will be used by GTE Sylvania to aid in checkout of the completed DCE. This test set is considered as a non-recurring cost and is not included in the unit production cost estimate.

The unit production cost estimates do not include other non-recurring engineering costs such as preparation of documentation, drawings, schematics, manufacturing assembly drawings, manufacturing assembly procedures, and test plans, DCE System checkout procedures and DCE performance specifications.

## 9.5 REDUNDANCY CONSIDERATIONS

A high degree of hardware redundancy is required in order to meet the stringent availability requirement imposed on the DCE in Section 4.6. However, extensive redundancy would not be required in most network applications due to the increased channel availability that would derive from the diversity routing capability of the DCE. In most practical situations, the DCE channel availability required would fall between the two cases discussed in Section 7.4, which are as follows:

- a. A basic DCE design - employs redundancy within the data memories and framing unit and provides channel availabilities of 0.999857 and 0.999809 for the IRGA/CEG and IRGB/CEG equipment configurations, respectively.
- b. Additional redundancy design - employs almost total hardware redundancy on a 1 for N basis and provides channel availabilities of 0.9999971 and 0.9999972 for the IRGA/CEG and IRGB/CEG equipment configurations, respectively.

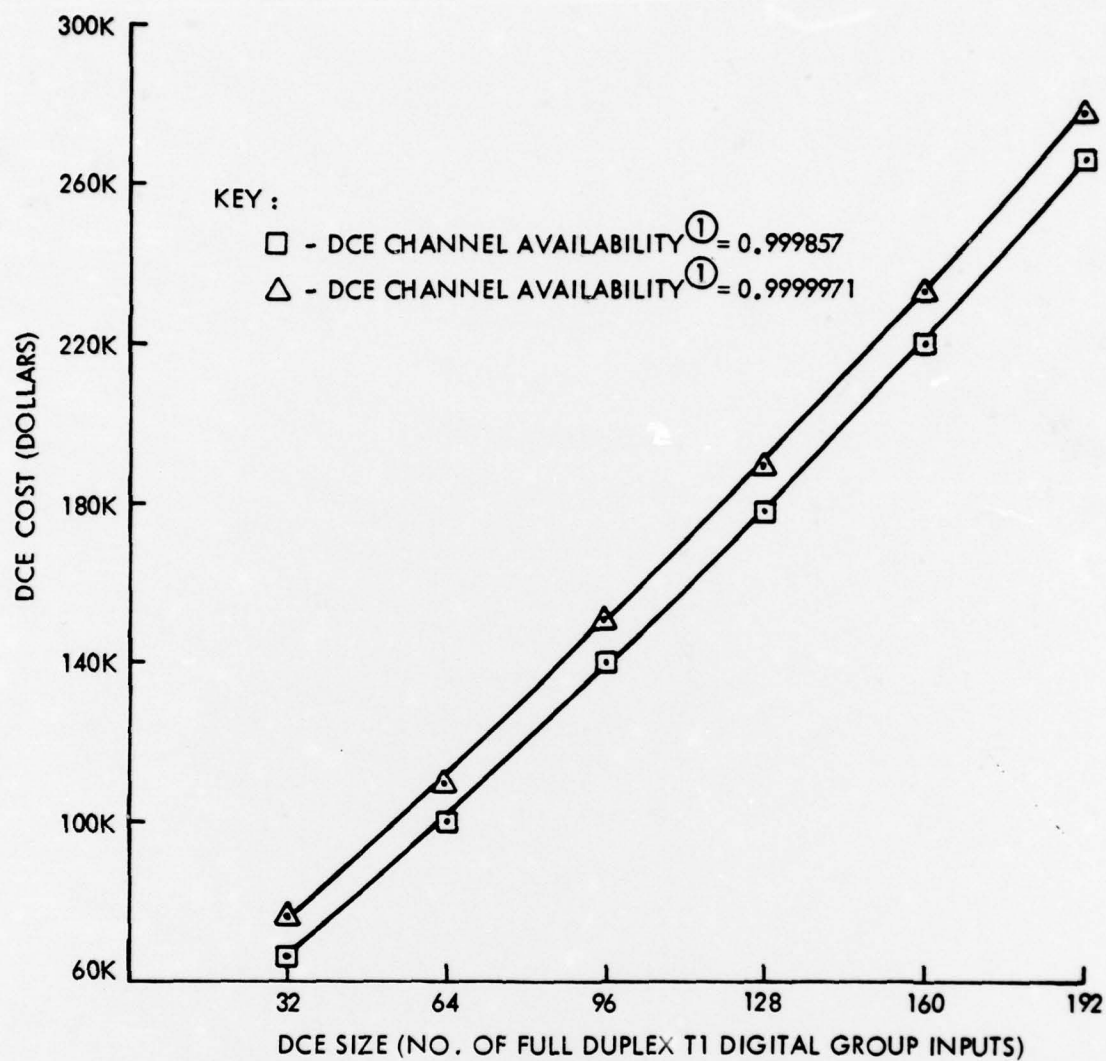
Production costs will be provided for the above two cases. This simplifies DCE costing for various applications since DCE costs for different availability requirements can be approximately linearly extrapolated from the two cases provided.

## 9.6 SUMMARY OF DCE PRODUCTION COSTS

Figure 9-1 provides a unit production cost summary for each size IRGA/CEG configuration. Figure 9-2 provides a unit production cost summary for each size IRGB/CEG configuration. The unit production costs for DCE configurations utilizing both IRGA and an IRGB may be determined from Figure 9-1 and 9-2 as follows:

- a. Determine unit production cost of the IRGA and CEG from Figure 9-1
- b. Determine unit production cost of the IRGB and CEG from Figure 9-2
- c. Add a. and b. and subtract either \$8500 for the  $\square$  channel availability or \$12580 for the  $\Delta$  channel availability.



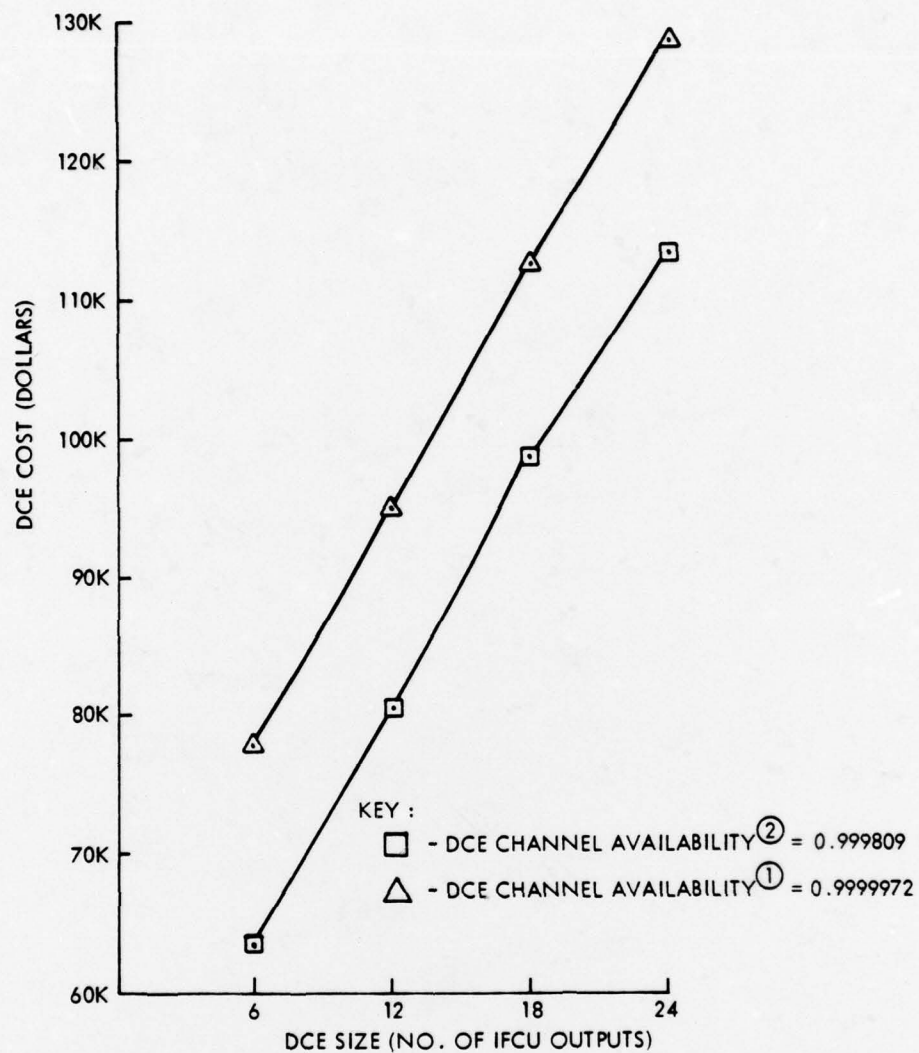


① SEE SECTION 9.5

3630-77E

Figure 9-1. DCE Cost Summary for IRGA and CEG Configuration





① SEE SECTION 9.5

② SEE SECTION 7.2.2.2.1

3631-77E

Figure 9-2. DCE Cost Summary for IRGB and CEG Configuration

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Block #20 (Cont'd)

3. Recommend the time frame for introducing DNC into the DCS.
4. Conceptually design DNC hardware and software elements based on a set of recommended functions and applications.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) The projected digital European Defense Communications System was used as a framework to achieve the following: 1. Identify and analyze digital network control (DNC) requirements. 2. Demonstrate by analysis that an automated and remotely controllable channel reassignment capability is the optimal application of DNC with respect to functional requirements. <i>A/over</i>		

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